MZ-E30

SERVICE MANUAL

US Model
Canadian Model
AEP Model
UK Model
E Model
Australian Model
Tourist Model

Model Name Using Similar Mechanism	NEW
Mini Disc Mechanism Type	MT-MZE30-126
Tape Transport Mechanism Type	ODX-1

SPECIFICATIONS

System

Audio playing system
MiniDisc digital audio system
Laser diode properties
Material: GaAlAs
Wavelength: l = 790 nm
Emission duration: continuous
Laser output: less than 44.6 µW
(This output is the value measured at a distance of 200 mm from the lens surface on the optical pick-up block.)
Revolutions
400 rpm to 900 rpm (CLV)
Error correction
Advanced Cross Interleave Reed Solomon Code (ACIRC)
Sampling frequency
44.1 kHz
Coding
Adaptive TRansform Acoustic Coding (ATRAC)
Modulation system
EFM (Eight to Fourteen Modulation)
Number of channels
2 stereo channels
1 monaural channel
Frequency response
20 to 20,000 Hz ± 3 dB
Wow and Flutter
Below measurable limit
Outputs
Headphones: stereo mini-jack, maximum output level 5 mW + 5 mW, load impedance 16 ohm

General

Power requirements
Sony AC Power Adaptor (not supplied) connected at the DC IN 1.5 V jack: 100–240V AC, 50/60 Hz
One size AA (LR6) battery (supplied)
Nickel metal hydride rechargeable battery NH-9WM(N) (supplied)
Batte.y operation time
See "Using on a dry battery"
Dimensions
Approx. 82 x 25.8 x 79.6 mm (w/h/d)
Mass
Approx. 120 g the player only
Approx. 160 g incl. a premastered MD, and a Ni.kel metal hydride rechargeable battery NH-9WM(N)
Supplied accessories
Battery Charger BC-7HT (1)
Rechargeable battery NH-9WM (N) (1)
Rechargeable battery carrying case (1)
Headphones with a remote controller (1)
Battery case (1)
Carrying case (1)
Ear pad (2)
Size AA (LR6) battery (1)

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Design and specifications are subject to change without notice.

PORTABLE MINI DISC PLAYER

MICROFILM

SONY®

CAUTION

Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Flexible Circuit Board Repairing

- Keep the temperature of the soldering iron around 270°C during repairing.
- Do not touch the soldering iron on the same conductor of the circuit board (within 3 times).
- Be careful not to apply force on the conductor when soldering or unsoldering.

Notes on Chip Component Replacement

- Never reuse a disconnected chip component.
- Notice that the minus side of a tantalum capacitor may be damaged by heat.

SAFETY-RELATED COMPONENT WARNING!!

COMPONENTS IDENTIFIED BY MARK ⚠ OR DOTTED LINE WITH MARK ⚠ ON THE SCHEMATIC DIAGRAMS AND IN THE PARTS LIST ARE CRITICAL TO SAFE OPERATION. REPLACE THESE COMPONENTS WITH SONY PARTS WHOSE PART NUMBERS APPEAR AS SHOWN IN THIS MANUAL OR IN SUPPLEMENTS PUBLISHED BY SONY.

ATTENTION AU COMPOSANT AYANT RAPPORT À LA SÉCURITÉ!

LES COMPOSANTS IDENTIFÉS PAR UNE MARQUE ⚠ SUR LES DIAGRAMMES SCHÉMATIQUES ET LA LISTE DES PIÈCES SONT CRITIQUES POUR LA SÉCURITÉ DE FONCTIONNEMENT. NE REMPLACER CES COMPOSANTS QUE PAR DES PIÈSES SONY DONT LES NUMÉROS SONT DONNÉS DANS CE MANUEL OU DANS LES SUPPÉMENTS PUBLIÉS PAR SONY.

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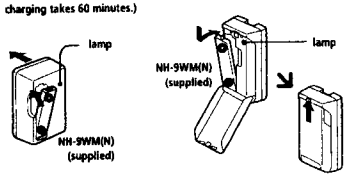
Playing an MD right away! A

Before Using the supplied rechargeable battery for the first time, charge it. Other choices are dry batteries and house current (see "Power sources").

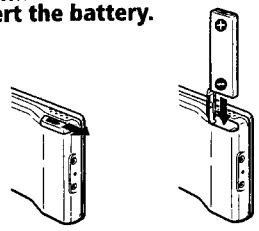
1 Charge the rechargeable battery.

Install the supplied rechargeable battery NH-9WM(N) to the supplied battery charger with correct polarity. And connect to wall outlet.
The charger lamp goes off when the chargings has finished.

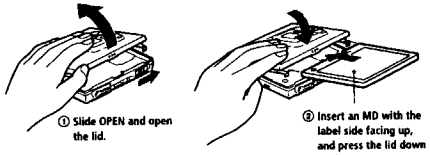
- **U.S.A., Canadian, European & Australian model (Full charging takes 60 minutes.)**
- **Other countries & World model (Full charging takes 120 minutes.)**



2 Insert the battery.



3 Insert an MD.



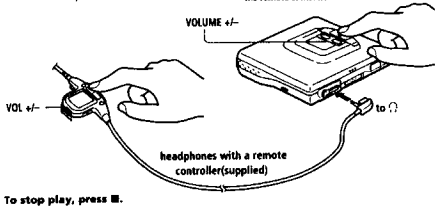
① Slide OPEN and open the lid.

② Insert an MD with the label side facing up, and press the lid down to close.

4 Play an MD.

① Press ►.
The player starts to play the first track. If you use remote controller, a short beep sounds in the headphones.

② Press VOLUME +/– (VOL +/– on the remote controller) to adjust the volume.
You can check the volume in the display of the remote controller.



To stop play, press ■.

To	Press (Beeps in the headphones)
Pause	❚❚ (Continuous short beeps) Press ❚❚ again to resume play.
Find the beginning of the current track	⏮ or ⏮ side of ► on the remote controller once (Three short beeps)
Find the beginning of the next track	⏭ or ⏭ side of ► on the remote controller once (Two short beeps)
Go backwards while playing[1]	keep pressing ⏮ or ⏮ side of ► on the remote controller
Go forward while playing[1]	keep pressing ⏭ or ⏭ side of ► on the remote controller
Remove the MD	■ and open the lid.[2]

If the play does not start
Make sure the player is not locked. See "To lock the controls."

For models supplied with the AC plug adaptor
If the battery charger does not fit the wall outlet, use the AC plug adaptor.

Display window while playing back

•Display window on the remote controller

•Display window on the player

1) To go backwards or forward quickly without listening, press ❚❚ and keep pressing ⏮ or ⏭.
2) Once you open the lid, the point to start play will change to the beginning of the first track.
3) Appears only with MDs that have been electronically labeled.

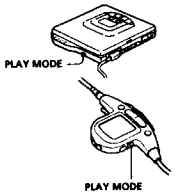
Note
Don't slide OPEN during playback. If you do, the lid will open and playback will stop.

The player automatically switches to play the stereo or monaural sound according to the recorded sound.

▶Various ways of playback

Playing tracks repeatedly B

You can play tracks repeatedly in three ways -all repeat, single repeat, and shuffle repeat.



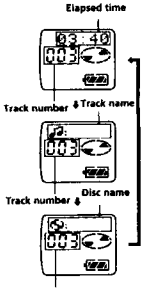
Press PLAY MODE while the player is playing an MD.
Each time you press PLAY MODE, the play mode indication changes as follows.

Play mode indication

(none) (normal play)
All the tracks are played once.
↓
" (all repeat)
All the tracks are played repeatedly.
↓
1" (single repeat)
A single track is played repeatedly.
↓
SHUF" (shuffle repeat)
All the tracks are played repeatedly in random order.

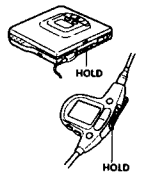
Tips on playback

To know the track name and time D
Press DISPLAY while the player is playing an MD.
Each time you press DISPLAY, the display changes as follows.



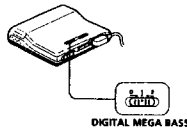
Note
Disc and track names appear only with MDs that have been electronically labeled.

To lock the controls B
To prevent the buttons from being accidentally operated when you carry the player, use this function.



Slide HOLD in the direction of the ➡.
On the player, slide HOLD to lock the controls of the player.

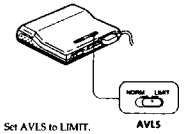
To emphasize bass (DIGITAL MEGA BASS) E
The DIGITAL MEGA BASS function intensifies low frequency sound for richer quality audio reproduction.



Slide DIGITAL MEGA BASS.
Choose 1 (slight effect) or 2 (strong effect). To cancel the effect, set DIGITAL MEGA BASS to 0.

Note
If the sound is distorted when emphasizing bass, turn down the volume.

To protect your hearing (AVLS) F
The AVLS (Automatic Volume Limiter System) function keeps down the maximum volume to protect your ears.



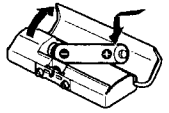
Set AVLS to LIMIT.
The volume is kept at a moderate level, even if you try to turn the volume above the limited level.

▶Power sources

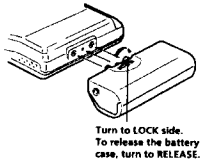
You can use the player on a dry battery, house current, or a Ni-MH rechargeable battery.

Using on a dry battery G

1 Insert one size AA (LR6) alkaline battery (supplied with the World model only) into the supplied battery case, and close the lid.



2 Attach the battery case to the player.



When to replace or charge the batteries
You can check the battery condition with the battery indication displayed while using the player.

- Used batteries
- Weak batteries. Replace all the batteries
- The batteries have gone out "LoBATT" flashes in the display, and the power goes off.

Battery life*

Batteries	Playback
Ni-MH rechargeable battery (NH-9WM(N))	Approx. 4 hours
One size AA (LR6) alkaline battery	Approx. 5 hours
One size AA(LR6) alkaline battery and a Ni-MH rechargeable battery (NH-9WM(N))	Approx. 10 hours

* The battery life may be shorter due to operating conditions and the temperature of the location.

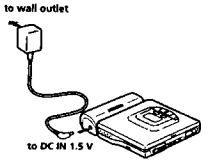
Using on house current H

Before using the player, remove the rechargeable battery if it is installed.

1 Attach the supplied battery case to the player.

2 Connect the AC-E15 L AC power adaptor (not supplied) to the DC IN 1.5V jack of the battery case.

3 Connect the AC power adaptor to wall outlet.



Note
The battery indication ▬ is displayed while using the AC power adaptor.

▶Additional information

Precautions

On safety
- Do not put any foreign objects in the DC IN 1.5 V jack.

On power sources
- Use the house current, one size AA (R6) battery, nickel metal hydride rechargeable battery, or car battery.
- For use in your house: Use the AC power adaptor AC-E15 L (not supplied). Do not use any other AC power adaptor since it may cause the player to malfunction.

Polarity of the plug

- The player is not disconnected from the AC power source (mains) as long as it is connected to the wall outlet, even if the player itself has been turned off.
- If you are not going to use this player for a long time, be sure to disconnect the power supply (AC power adaptor, dry batteries, rechargeable batteries, or car battery cord). To remove the AC power adaptor from the wall outlet, grasp the adaptor plug itself; never pull the cord.
- For use in the car: Use the CPA-9 car connecting pack and the DCC-E215 car battery cord(not supplied).

On charging
- Be sure to use the supplied battery charger.
- Charging time may vary depending on the battery condition.
- When you use the battery for the first time or after a long period of disuse, the battery life may be shorter. In this case, charge and discharge the battery several times. The battery life will be restored.
- If the rechargeable battery capacity becomes half the normal life, replace it with a new one.

On heat build-up
- Heat may build up in the player if it is used for an extended period of time. In this case, leave the player to cool down.

On installation
- Never use the player where it will be subjected to extremes of light, temperature, moisture or vibration.
- Never wrap the player in anything when it is being used with the AC power adaptor. Heat build-up in the player may cause malfunction or injury.

On the headphones
Road safety
Do not use headphones while driving, cycling, or operating any motorized vehicle. It may create a traffic hazard and is illegal in many areas. It can also be potentially dangerous to play your player at high volume while walking, especially at pedestrian crossings. You should exercise extreme caution or discontinue use in potentially hazardous situations.

Preventing hearing damage
Avoid using headphones at high volume. Hearing experts advise against continuous, loud and extended play. If you experience a ringing in your ears, reduce the volume or discontinue use.

Caring for others
Keep the volume at a moderate level. This will allow you to hear outside sounds and to be considerate of the people around you.

On the MiniDisc cartridge
- Do not break open the shutter.
- Do not place the cartridge where it will be subject to light, temperature, moisture or dust.

On cleaning
- Clean the player casing with a soft cloth slightly moistened with water or a mild detergent solution. Do not use any type of abrasive pad, scouring powder or solvent such as alcohol or benzene as it may mar the finish of the casing.
- Wipe the disc cartridge with a dry cloth to remove dirt.
- Dust on the lens may prevent the unit from operating properly. Be sure to close the disc compartment lid after inserting and ejecting an MD.

Notes on the batteries
Incorrect battery usage may lead to leakage of battery fluid or bursting batteries. To prevent such accidents, observe the following precautions:
- Install the + and – poles of the batteries correctly.
- Do not try to recharge the batteries.
- When the player is not to be used for a long time, be sure to remove the batteries.
- If a battery leak should develop, carefully and thoroughly wipe away battery fluid from the battery compartment before inserting new ones.

Note on mechanical noise
The player gives out mechanical noise while operating, which is caused by the power-saving system of the player and it is not a trouble.

SECTION 1
GENERAL

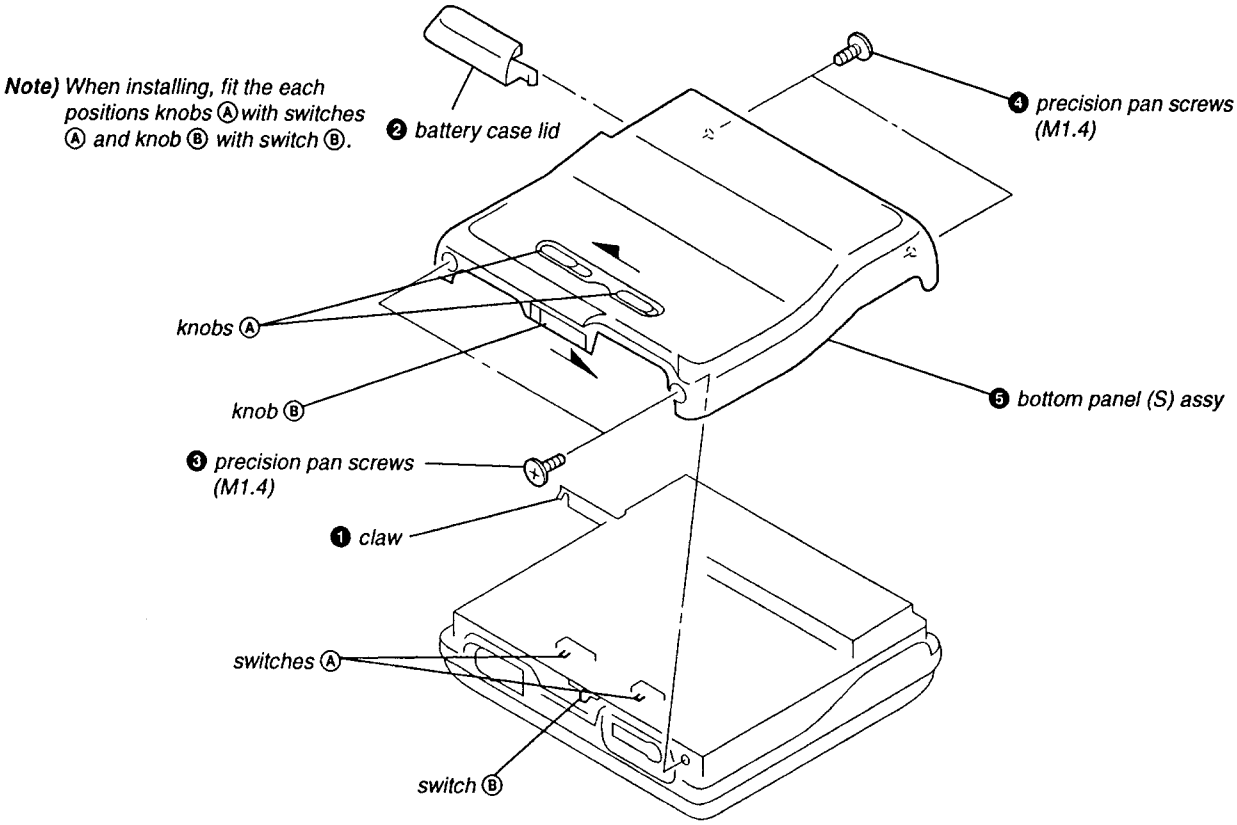
This section is extracted from instruction manual.

SECTION 2
DISASSEMBLY

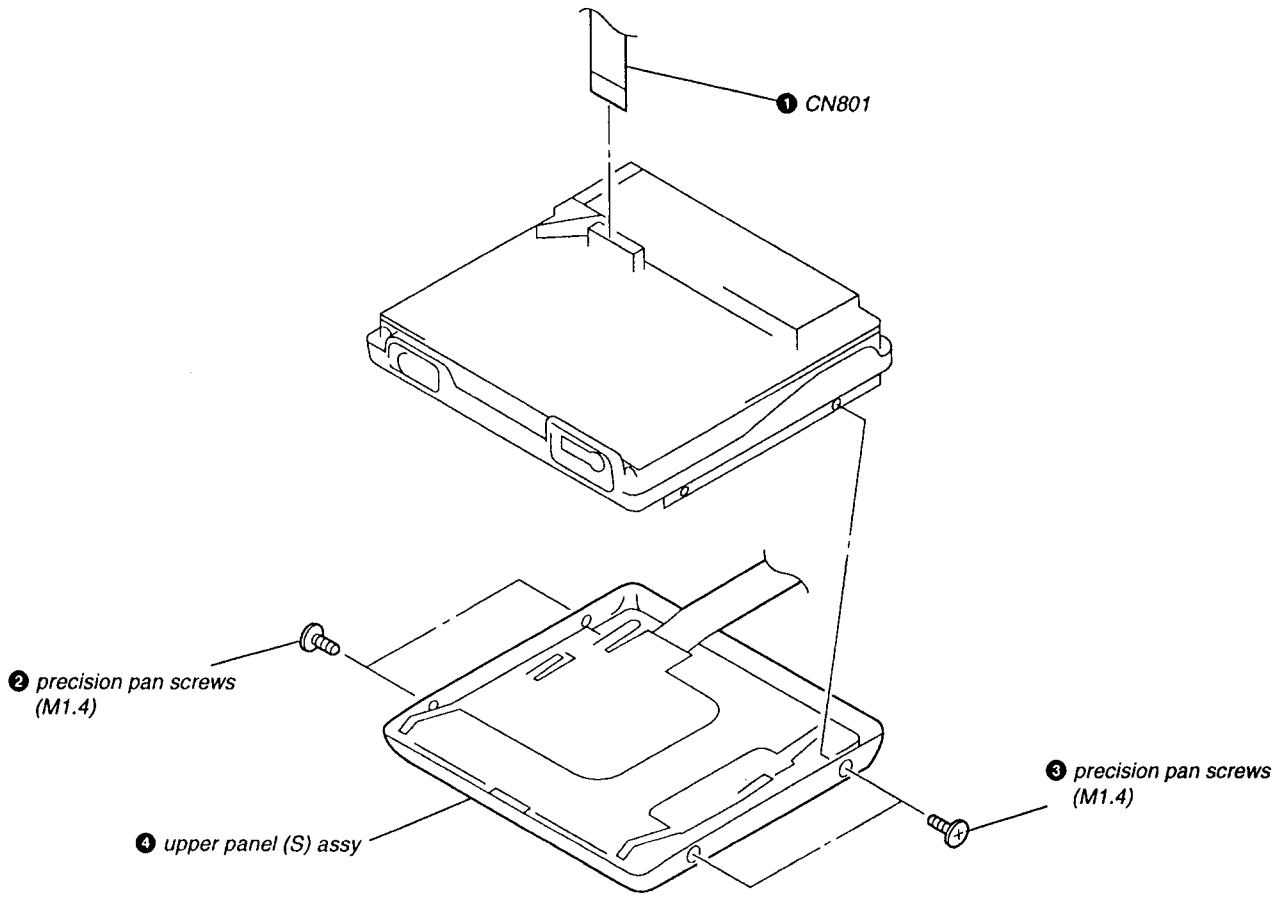
Note : This set can be disassemble according to the following sequence.
Bottom Panel (S) assy ➡ Upper Panel (S) assy ➡ Main Board ➡ Belt assy ➡ Chassis (Belt) assy ➡ Optical Pick-up Block

Note : Follow the disassembly procedure in the numerical order given.

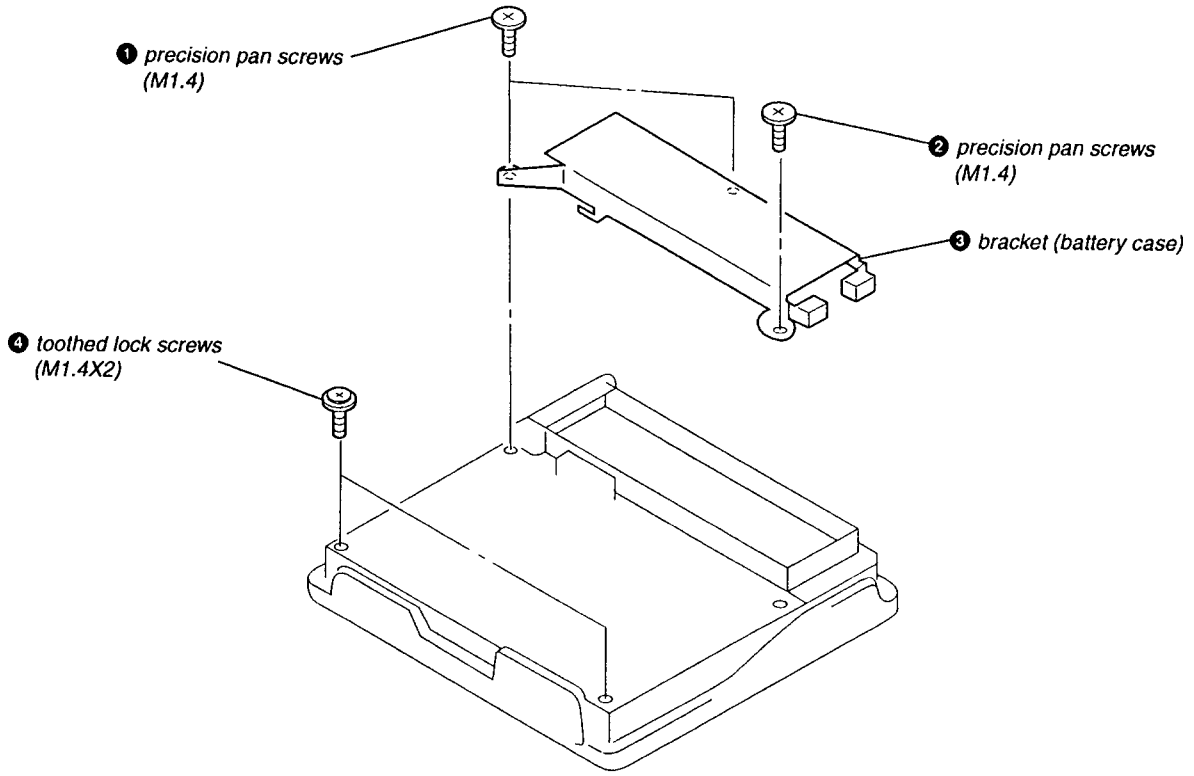
2-1. BOTTOM PANEL (S) ASSY

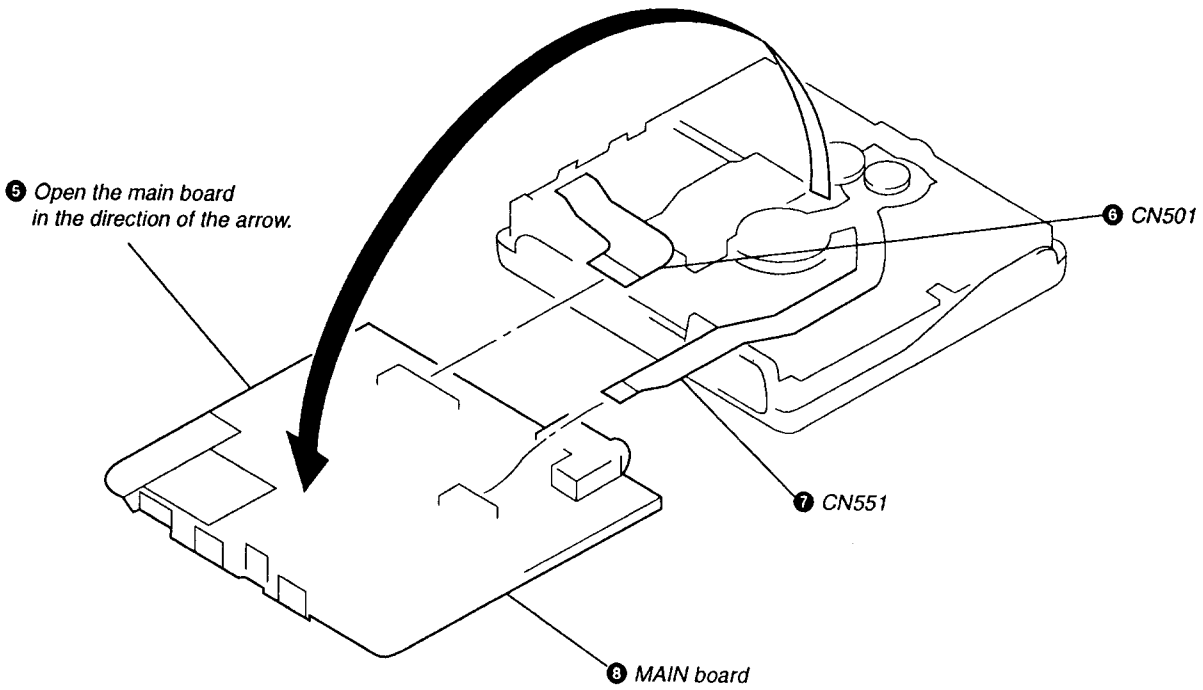

Note) When installing, fit the each positions knobs Ⓐ with switches Ⓐ and knob Ⓑ with switch Ⓑ.
❷ battery case lid
❹ precision pan screws (M1.4)
knobs Ⓐ
knob Ⓑ
❺ bottom panel (S) assy
❸ precision pan screws (M1.4)
❶ claw
switches Ⓐ
switch Ⓑ

2-2. UPPER PANEL (S) ASSY

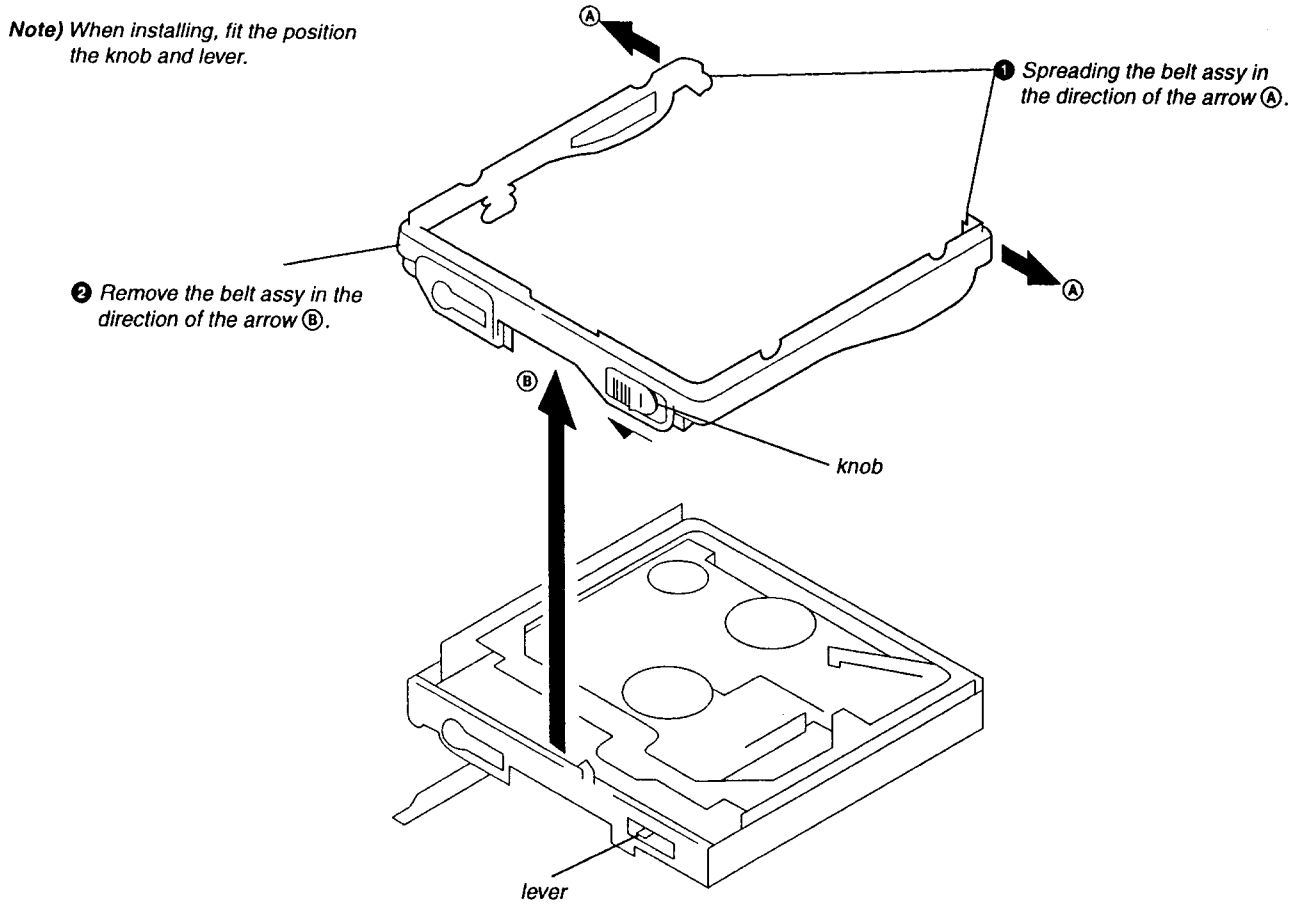


2-3. MAIN BOARD

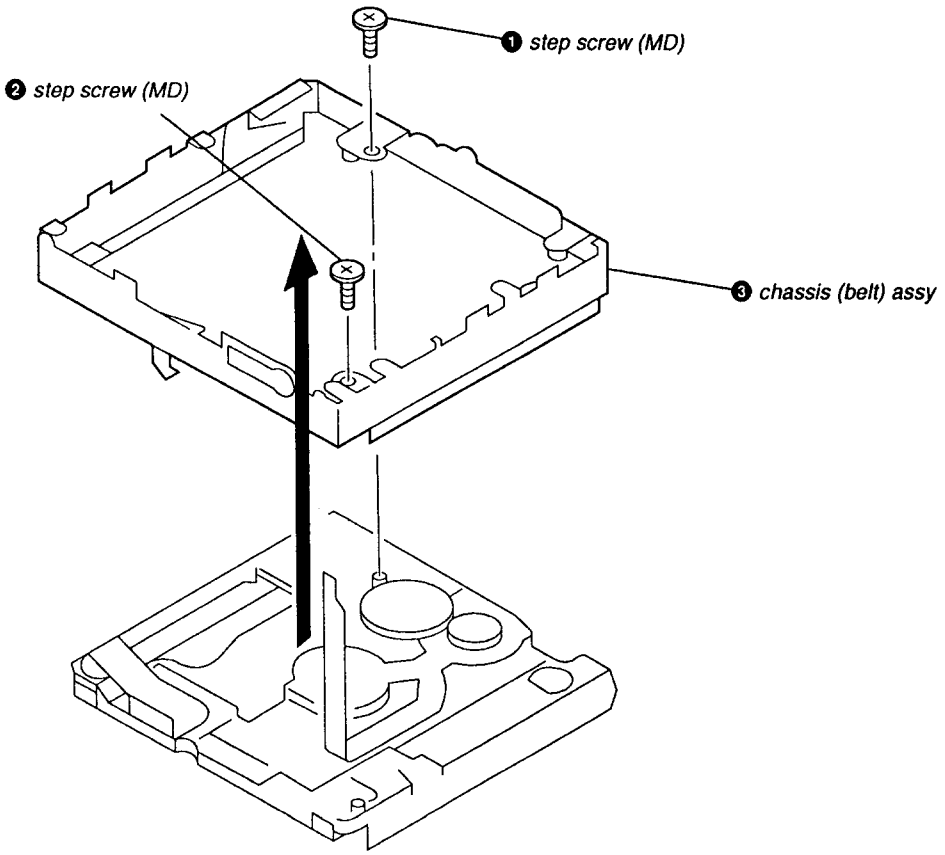




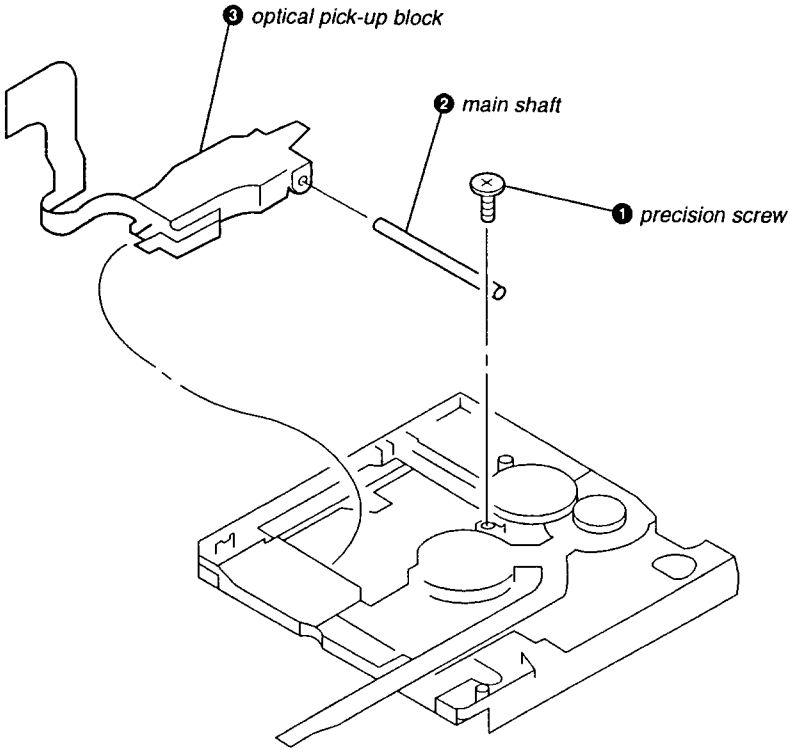
2-4. BELT ASSY


Note) When installing, fit the position the knob and lever.
❶ Spreading the belt assy in the direction of the arrow Ⓐ.
❷ Remove the belt assy in the direction of the arrow Ⓑ.
knob
lever

2-5. CHASSIS (BELT) ASSY



2-6. OPTICAL PICK-UP BLOCK



SECTION 3
TEST MODE

Outline

- In this set, overall adjustment mode is made available by entering test mode to perform automatic adjustment of CD and MO.
  In the overall adjustment mode, the disc is determined whether it is CD or MO and adjustments are performed in sequence. If a fault is found, the location of the fault is displayed. Also, in servo mode, each adjustment can be automatically made.

Setting the Test Mode

To enter the test mode, two methods are available :

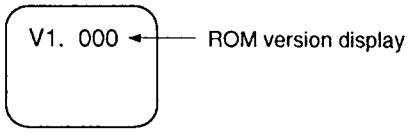
1. Entering method with key input
   Turn on the HOLD switch on the set. While holding down the ■ key on the set, press the following keys in the following order :
   ▶▶| → ▶▶| → |◀◀ → |◀◀ → ▶▶| → |◀◀ → ▶▶| → |◀◀ → ❚❚ → ❚❚
2. Entering method by shorting the test point
   Solder bridge the test point TAP801 (TEST) on the main board (connect IC801 pin ㉜ to GND), and turn on the POWER.

Releasing the Test Mode

1. When test mode was entered with key input, turn off the POWER.
2. When test mode was entered by shorting the test point, turn off the POWER and open the solder bridge of TAP801 (TEST) on the main board.

Operation of Setting on Test Mode

When the test mode is set, the LCD displays the following :

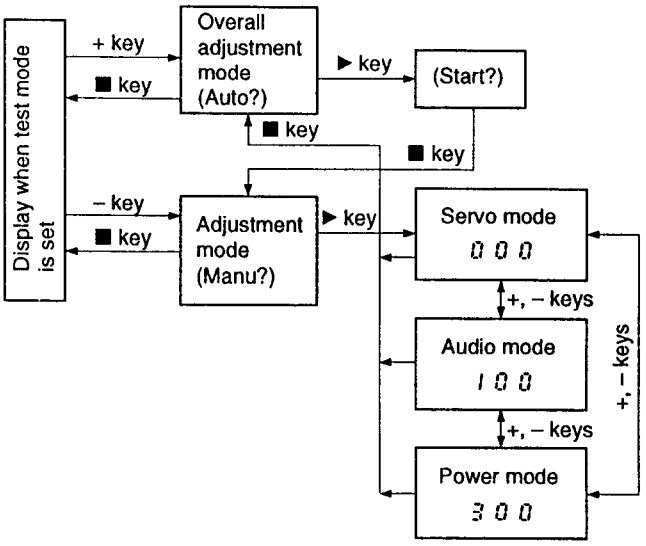


LCD on remote commander

- ROM version display to all LEDs ON to all LEDs OFF and so on. These operations are repeated.
- When the PLAY MODE key is pressed and hold down, the display at that time is held so that the display can be checked.

Configuration of Test Mode

The test mode has the configuration given below.

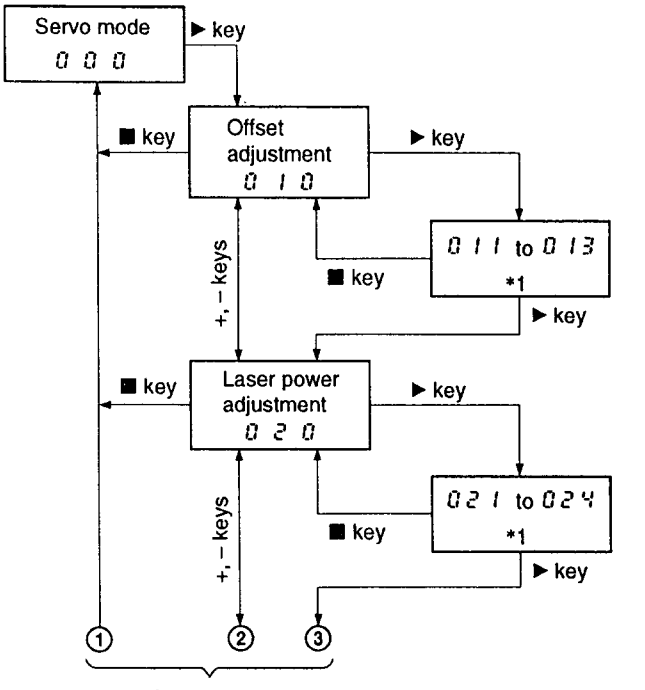


Displays of the LCD on the remote commander are shown in parentheses.

Servo Mode

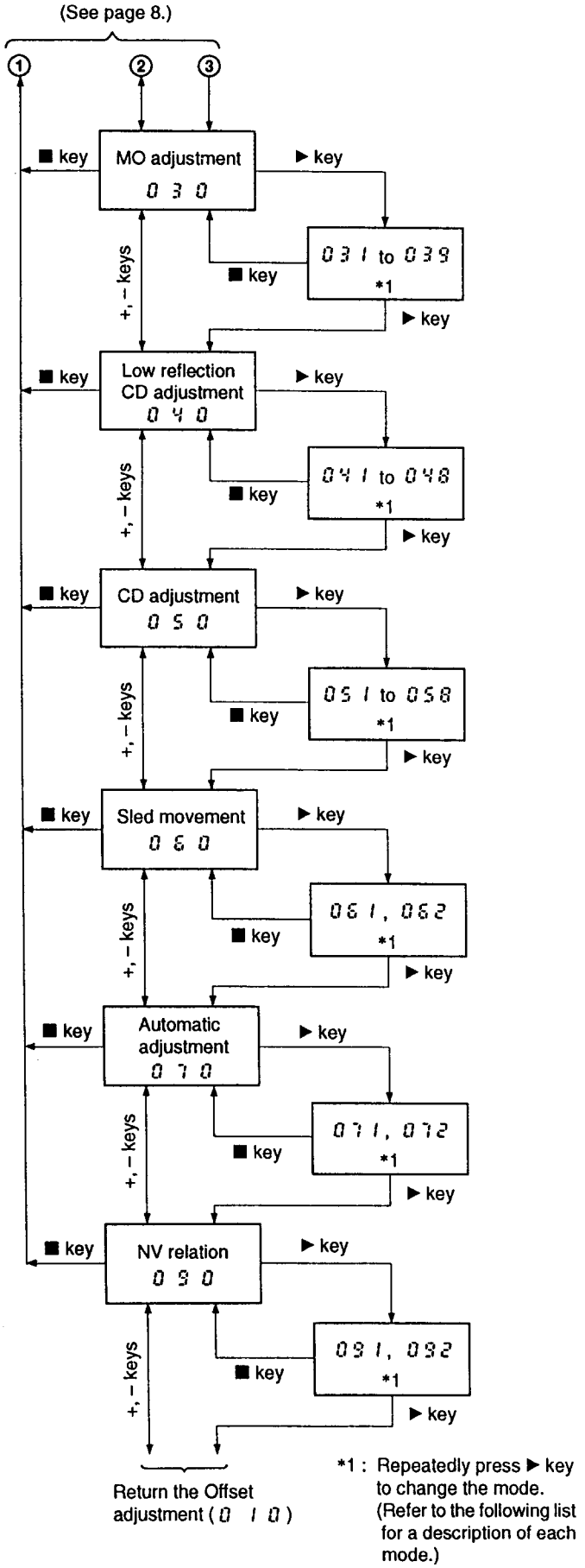
- Set the test mode, press the VOLUME – key and use the ▶ key to set the servo mode.
- When the servo mode is set, use the ▶▶| key and the |◀◀ key to move the optical pick-up to the outer circumference and to the inner circumference respectively.
- When entering another mode, refer to the configuration of test mode.

1. Structure of Servo Mode



(See page 9.)

*1 : Repeatedly press ▶ key to change the mode. (Refer to the following list for a description of each mode.)



2. Description of Each Mode

0 10 Offset adjustment

Mode	Description
0 11	FE offset
0 12	TE offset
0 13	All servo ON

020 Laser power adjustment

Mode	Description
021	MO power A
022	MO power E
023	CDL power
024	CD power

030 MO adjustment

Mode	Description
031	MO EF balance
032	MO EF gain
033	MO ABCD gain
034	MO focus gain
035	MO tracking gain
036	MO RF gain
037	MO ADIP gain
038	MO focus bias E
039	MO focus bias A

040 Low reflection CD adjustment

Mode	Description
041	Low reflection CD EF balance
042	Low reflection CD EF gain
043	Low reflection CD ABCD gain
044	Low reflection CD focus gain
045	Low reflection CD tracking gain
046	Low reflection CD RF offset
047	Low reflection CD RF gain
048	Low reflection CD focus bias

050 CD adjustment

Mode	Description
051	CD EF balance
052	CD EF gain
053	CD ABCD gain
054	CD focus gain
055	CD tracking gain
056	CD RF offset
057	CD RF gain
058	CD focus bias

060 Sled movement

Mode	Description
061	Sled in
062	Sled out 5

070 Automatic adjustment

Mode	Description
071	Focus search
072	Access 32
073	ADER check

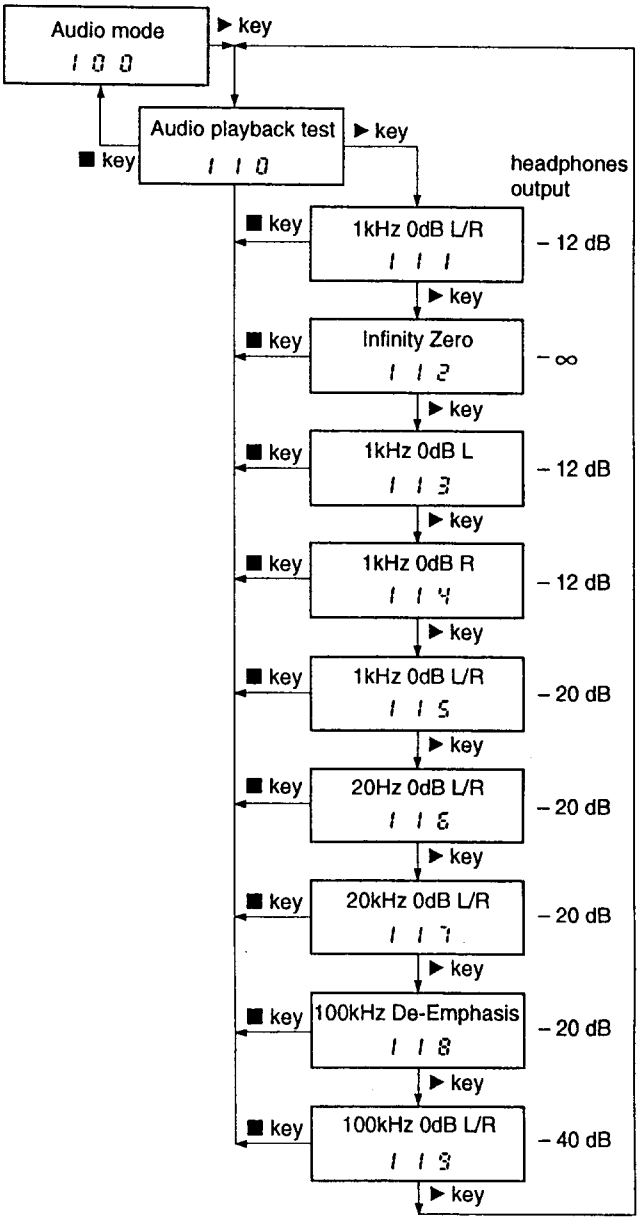
090 NV relation

Mode	Description
091	NV clear
092	Power OFF

Audio Mode

- Enter the test mode and press the VOLUME – key. Then, press the ▶ key and the VOLUME + key in this turn to enter audio mode.
- When entering another mode, refer to the configuration of test mode.

1. Structure of Audio Mode



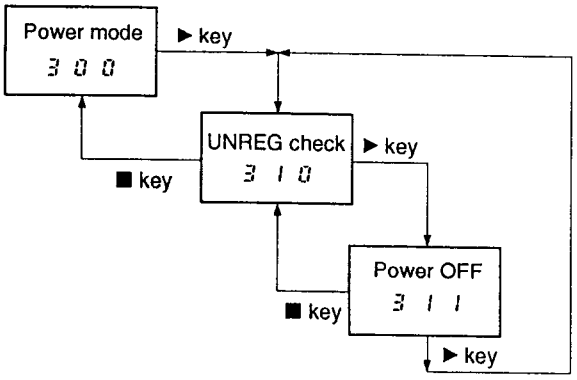
- The mode No. 111 is for S/N and crosstalk. The mode No. 115 is for distortion factor and frequency characteristics.
- When the VOLUME +/– keys is pressed in any mode, the volume of the headphones is changed (increased/decreased) in units of one step. When the ▶▶I / I◀◀ keys is pressed, the volume of the headphones is maximized/minimized.
- For the volume value, any changed value remains as it is basically. However, when the volume is switched from 114 to 115 or 118 to 119, it returns the default value.

SECTION 4
ELECTRICAL ADJUSTMENTS

Power Mode

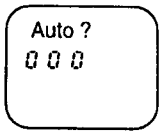
- Enter the test mode and press the VOLUME – key. Then, press the ▶ key and the VOLUME – key in this turn to enter power mode.
- When entering another mode, refer to the configuration of test mode.

1. Structure of Power Mode

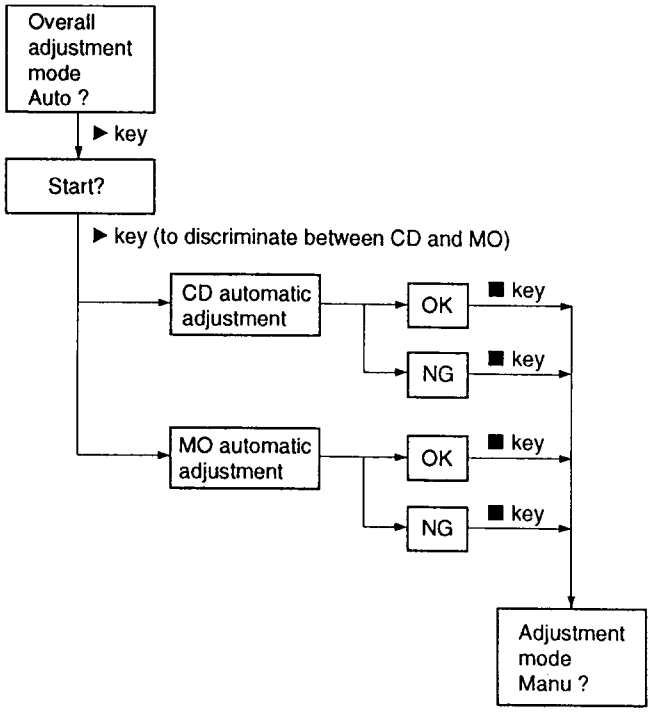


Overall Adjustment Mode

- Enter the test mode and press the VOLUME + key to enter overall adjustment mode.
- When entering another mode, refer to the coufiguration of test mode.
- When the overall adjustment mode is entered, the LCD on the remote commander displays the following :



1. Structure of Overall Adjustment Mode



Notes for Adjustment

- In this set, automatic adjustment of CD and MO can be performed by entering the test mode.
- Adjustments are performed in the overall adjustment mode. If an item is determined as NG, the item is readjusted in servo mode.

Adjustment Method in Overall Adjustment Mode

1. Enter the test mode and press the VOLUME + key to enter overall adjustment mode.
2. Insert the CD test disc (TGYS-1) or SONY MO disc (recorded) commercially available.
3. Press the ▶ key twice. The disc is determined whether it is CD or MO and each adjustment mode is set. Automatic adjustments are performed in the order of the items listed below.

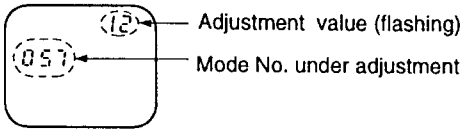
- In CD Automatic Adjustment Mode

No.	Mode	Description
1	0 8 1	Sled in
2	0 7 1	Focus search
3	0 8 2	Sled out 5
4	0 5 1	CD EF balance
5	0 5 2	CD EF gain
6	0 5 1	CD EF balance
7	0 5 3	CD ABCD gain
8	0 5 4	CD focus gain
9	0 5 5	CD tracking gain
10	0 5 6	CD RF offset
11	0 5 7	CD RF gain
12	0 5 6	CD RF offset
13	0 5 8	CD focus bias

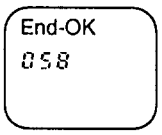
• In MO Automatic Adjustment Mode

No.	Mode	Description
1	061	Sled in
2	071	Focus search
3	062	Sled out
4	031	MO EF balance
5	032	MO EF gain
6	031	MO EF balance
7	033	MO ABCD gain
8	034	MO focus gain
9	035	MO tracking gain
10	036	MO RF gain
11	037	MO ADIP gain
12	038	MO focus bias E
13	039	MO focus bias A
14	013	ADER check
15	061	Sled in
16	071	Focus search
17	041	Low reflection CD EF balance
18	042	Low reflection CD EF gain
19	041	Low reflection CD EF balance
20	043	Low reflection CD ABCD gain
21	044	Low reflection CD focus gain
22	045	Low reflection CD tracking gain
23	046	Low reflection CD RF offset
24	047	Low reflection CD RF gain

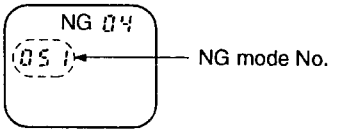
* Remote commander display during automatic adjustment



4. If result of automatic adjustment is OK, the following display appears.



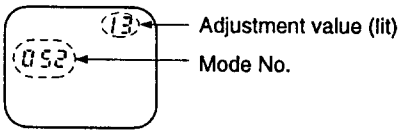
5. If result of automatic adjustment is NG, the following display appears.



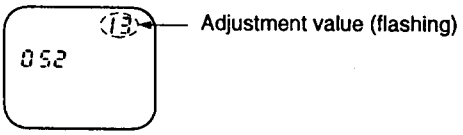
* If NG, enter servo mode to perform automatic adjustment of the item determined as NG.

Adjustment in Servo Mode Method

1. When each adjustment mode is set according to the structure of servo mode, the lower two digits of the mode No. and the adjustment value written in EEPROM are displayed and lit on the LCD on the remote commander.

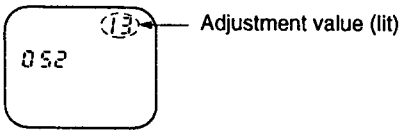


2. When the ▮▮ key is pressed, the following display appears and the automatic adjustment is performed.



Note) Although the VOLUME +/– keys can be used to change the adjustment value to any value, they should not be used whenever possible.

3. When the automatic adjustment is completed, the flashing adjustment value is lit.



SECTION 5
DIAGRAMS

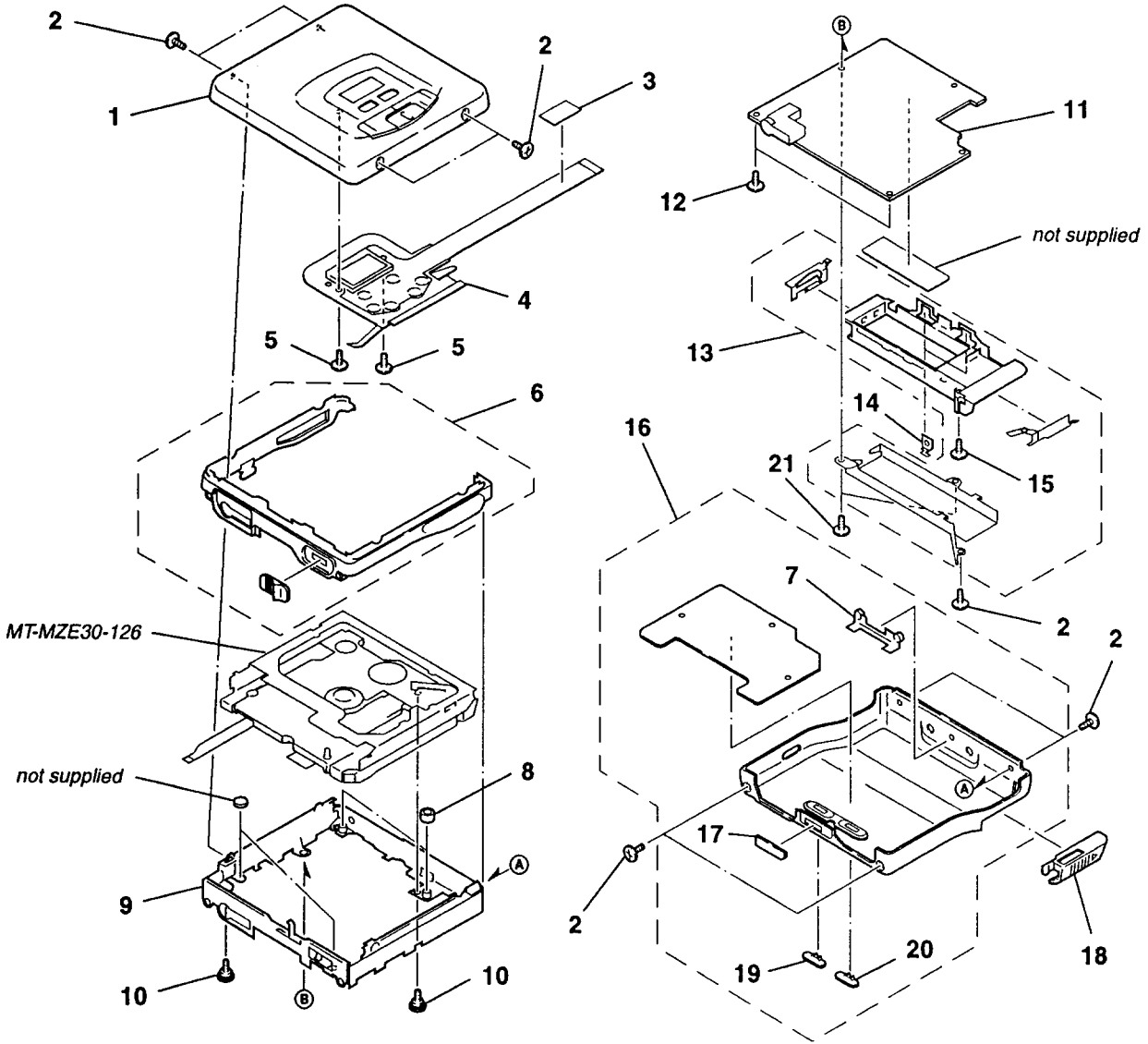
5-1. IC PIN DESCRIPTION

- **IC801 RU6715TF-0003 (SYSTEM CONTROL)**

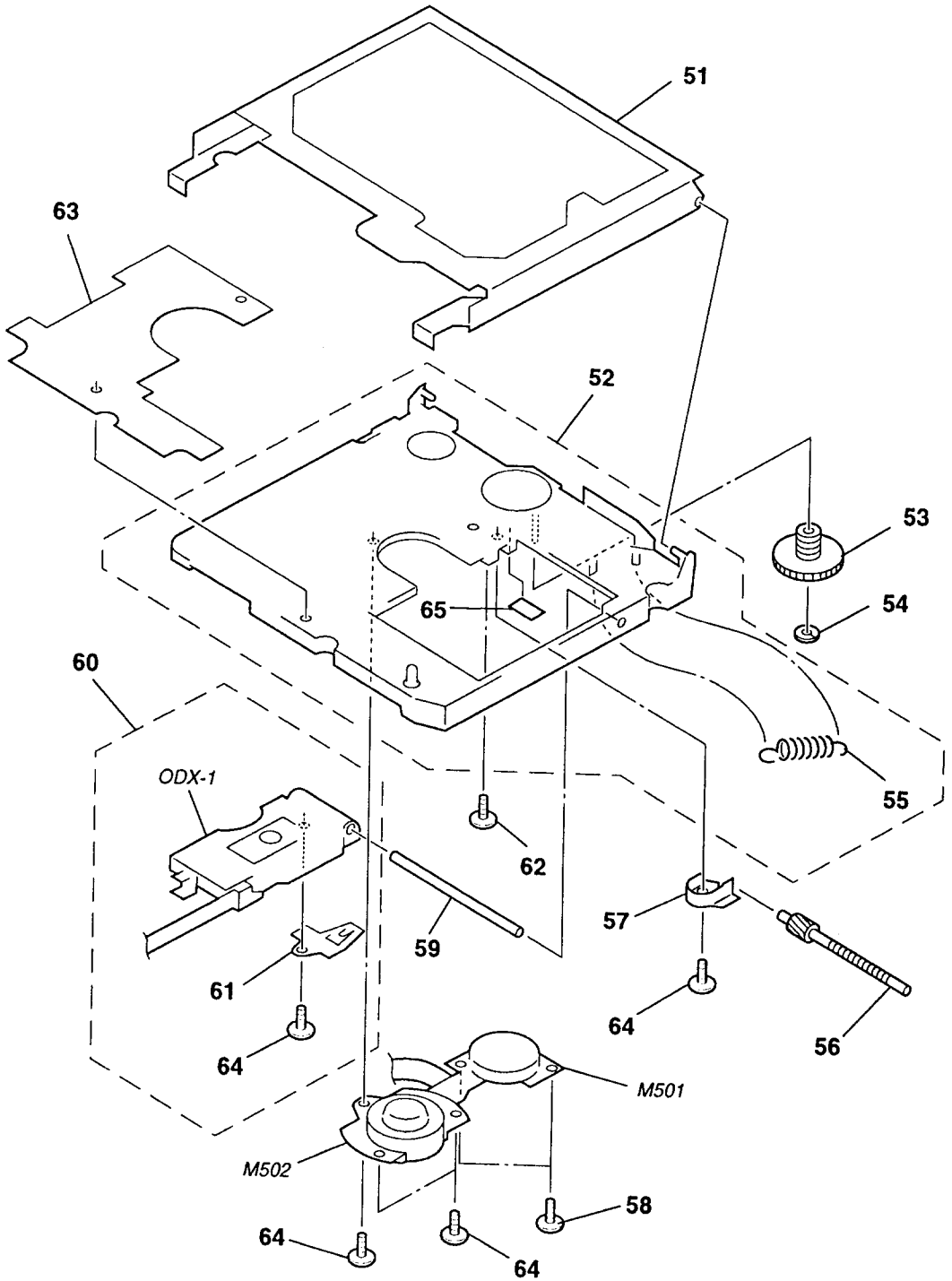
Pin No.	Pin Name	I/O	Pin Description
1	CHG MON	—	Not used. (Fixed at "L".)
2	UREG MON	I	Unreg voltage monitor input
3	VTEMP	I	Temperature sensor input
4	VREF	I	Reference voltage monitor input
5	PLAY KEY	I	Set PLAY key input
6	OPN CLS SW	I	OPEN/CLOSE switch input
7	RMC KEY	I	Remote commander key input
8	SET KEY	I	Set key input
9	XRESET	I	System reset input (At reset : "L")
10	AVDD	—	A/D converter power supply
11	AVSS	—	A/D converter GND
12, 13	NC	—	Not used.
14	HOLD SW	I	Set HOLD switch input
15	(REFLECT)	—	Not used. (Fixed at "H".)
16	NC	—	Not used.
17	VREG CON	—	2.5 V voltage on/off switch
18	XWK CLR	O	Power IC wakeup factor latch clear output and motor driver IC control signal output
19	SLEEP	O	System sleep output
20	MCK	I	Master clock input
21	NC	—	Not used.
22	VDD	—	Digital power supply
23	VSS	—	Digital GND
24	NC	—	Not used.
25	VSS	—	Digital GND
26	UREG CHK CON	O	Unreg voltage monitor control output
27	DSP SINT	I	Interrupt input from DSP.
28	NC	—	Not used.
29	AVLS SW	I	Set AVLS switch input
30, 31	NC	—	Not used.
32	ADJUST	I	Normally, Test mode select input. ("L" : Test mode)
33	NC	—	Not used.
34	SBUS CLK	O	SBB serial clock output
35	SBUS DATA	O	SBB serial data output
36	FR CAP	—	Free-run counter capture input (Not used.)
37	SLD 1 MON	I	Sled servo timing signal input
38	SLD 2 MON	I	Sled servo timing signal input
39	CLV VCON	O	Spindle servo drive voltage control output
40	V28 CON	O	Power voltage correction control output
41	APC REF	O	Laser power control output
42	CLV U MON	I	Spindle servo timing signal input
43	CLV V MON	I	Spindle servo timing signal input
44	CLV W MON	I	Spindle servo timing signal input
45	CLV U CON	O	Spindle servo drive signal output
46	CLV V CON	O	Spindle servo drive signal output
47	CLV W CON	O	Spindle servo drive signal output
48	NC	—	Not used.
49	FR TRG	—	Free-run counter capture output (Not used.)
50	VDD	—	Digital power supply
51	VPP	—	Power for on board light.

Pin No.	Pin Name	I/O	Pin Description
52	VSS	—	Digital GND
53	SLD 1R CON	O	Gate array control signal output
54	SLD 1F CON	O	Gate array control signal output
55	SLD 2R CON	O	Gate array control signal output
56	SLD 2F CON	O	Gate array control signal output
57 – 59	SLD DLY4 – 6	O	Gate array control signal output
60	SLED MODE	O	Gate array control signal output
61	SPCK	O	TSB serial clock output
62	RMC DTCLK	I/O	TSB serial data input/output
63 – 65	NC	—	Not used.
66	SLED DIR	O	Gate array control output
67	SLD VCON	O	Sled servo outer voltage control output
68	SLD PWR UP	O	Bypass transistor control output for sled drive power supply.
69	HP MUTE	O	Headphone amplifier mute output
70	HP STBY	O	Headphone amplifier standby output
71	RMC SEL	O	TSB/SSB select signal output for remote commander terminal.
72	NV DO	O	Serial data signal output for NVRAM.
73	NV DI	I	Serial data signal input from NVRAM.
74	NV CLK	O	Serial clock signal output for NVRAM.
75	NV CS1	O	Chip select signal output for NVRAM.
76	VDD	—	Digital power supply
77 – 79	LCD VL2 – 0	—	LCD drive level power supply
80	VSS	—	Digital GND
81 – 87	NC	—	Not used.
88 – 96	LCD SEG0 – 8	O	LCD segment terminal
97 – 100	LCD COM0 – 3	O	LCD common terminal

6-1. PANEL SECTION



6-2. MD SECTION (MT-MZE30-126)



NEW TECHNICAL THEORY FOR SERVICING

MZ-E30
OPERATION MANUAL

PORTABLE MINI DISC PLAYER

SONY®

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2. FUNCTIONS AND FEATURES

The MZ-E30 has a pickup mass reduced by about 80% and thickness reduced by about 30% as compared with the conventional player (Model MZ-E3). With a newly developed LSI employed, the MZ-E30 also has less component parts by 45% while decreasing the power consumption by half or more. In addition, the MZ-E30 is the first Mini Disc available in the industry that can be driven with one rechargeable battery, thereby realizing both compact size and light weight.

The MZ-E30 comes in a pop design with dazzling colors, whose special coating causes the color tone to change delicately according to the angle of division in a small size similar to the jacket of a recording Mini Disc.

Table 2-1. shows the principal difference in Mini Discs for the exclusive use of playback by generation.

Table 2-1. Principal Difference in Mini Discs for Playback's Exclusive Use

	1st Generation	2nd Generation	3rd Generation	4th Generation
Model No.	**MZ-2P**	**MZ-E2**	**MZ-E3**	**MZ-E30**
Month/Year of Release	DEC/92	MAR/94	SEP/95	APR/97
Outside Dimensions (width x height x depth) (mm)	114 x 42 x 139	106.8 x 18.5 x 74	116 x 19.9 x 74	82 x 25.8 x 79.6
Mass (weight)	Approx. 680g (including the rechargeable battery)	Approx. 170g (body only)	170g (body only)	120g (body only)
Power Supply Voltage	6.0V	6.0V	3.0V	1.5V
Dry Battery Employed	x	AA battery x 3 (with battery housing required)	AA battery x 2	AA battery x 1 (with battery housing required)
Rechargeable Battery (attached)	BP-MZ1 (nickel-cadmium)	LIP-10 (lithium-ion)	BP-DM20 (nickel hydrogen)	BP-9WM(N) (nickel hydrogen)
Battery Power Supply Duration: Rechargeable battery	Approx. 1.25 hours	Approx. 2 hours	Approx. 3 hours	Approx. 4 hours
Battery Power Supply Duration: Dry battery (alkaline)	x	Approx. 4 hours	Approx. 4 hours	Approx. 5 hours
Liquid Crystal Display (LCD)	Body only	Remote control only	Body + Remote control	Body + Remote control
Number of Digits Displayable	12 (capable of being scrolled)	6 (capable of being scrolled)	6 (capable of being scrolled)	6 (capable of being scrolled)

2-1. Principal Features

[MZ-E30]

- Employing an impactive compact and lightweight jacket.
- Driven at 1.5 volts with an attached hydrogen rechargeable battery (NH-9WM(N)).
- Capable of being mounted with another dry battery in the attached housing externally fitted. Even if the rechargeable battery has used out, the MZ-E30 assures reliability since it is operative with one dry battery.
- Allowing the MZ-E30 to play back for about four consecutive hours with a rechargeable battery and for about five hours with one AA alkaline dry battery. With both jointly employed, the MZ-E30 is capable of playing back for about ten consecutive hours.
- Permitting the rechargeable battery to be charged fully in about one hour with the attached quick battery charger (BC-7HT).
- Applicable to a vehicle power supply by way of a dry battery housing.
- Capable of displaying doubly with liquid crystals in both body and remote commander.

3. DIFFERENCE IN SYSTEM CONFIGURATIONS BY GENERATION

For a Mini Disc of playback type, each system is composed of such principal LSIs as shown in **Table 3-1.**. The difference between the first and second generations lies in the L/Rch, two pieces of which have been employed in the ATRAC decoder of the first generation and are intensified into a single LSI in the second generation. The third generation, moreover, has had the principal LSIs intensified into three pieces except for the servo driver as shown in the table.

In the fourth generation, on the other hand, has been far larger sized and more highly integrated. As a result, the principal circuit of a Mini Disc has been intensified into a single LSI while six LSIs, including the ATRAC decoder, were employed in the first generation.

In the case of a playback type model heretofore available, a playback circuit and a decoder circuit have been employed while jointly using the principal LSI with a recorder/playback unit. The MZ-E30, however, employs an newly developed LSI for the exclusive use of playback, which has especially main functions, such as shock-proof, ATRAC decoding, EFM decoding and ACIRC decoding.

The principal LSI in the fourth generation are outlined below.

µPD63730GC : DSSP (digital servo): EFM decoder, ACIR decoder, DRAM controller, ADIP decoder, and clock generator circuit
MPC17A55FTA : Servo drive circuit, and step up/down power supply circuit
SN761050A : RF amplifier, and I-V amplifier with a gain adjustment switch

Table 3-1. Principal LSIs Employed in a Mini Disc for Playback

Applicable Model / Circuit Block	1st Generation	2nd Generation	3rd Generation	4th Generation
	MZ-2P	MZ-E2	MZ-E3 MZ-E40	MZ-E30
ATRAC Decoder	CXD2527R(2)	CXD2531AR	CXD2536R	µPD63730GC
Shock-proof Memory Controller	CXD2526Q	CXD2526AR		
EFM ACRIC Decoder	CXD2525R	CXD2525R	CXD2535BR	
ADIP Demodulator	CXA1380N	CXA1380N		
Servo Signal Processor	CXA1602R	CXA1602R		
Servo Driver	MPC1718PU	MPC1718PU	MPC17A38VM	MPC17A55FTA
RF Amplifier	CXA1381R	CXA1861R	CXA1981AR	SN761050A

3-1. System Block Diagrams

The playback type Mini Discs belonging to the first thru 4th generations have their respective systems composed of the blocks illustrated below.

(1) 1st Generation [MZ-2P]

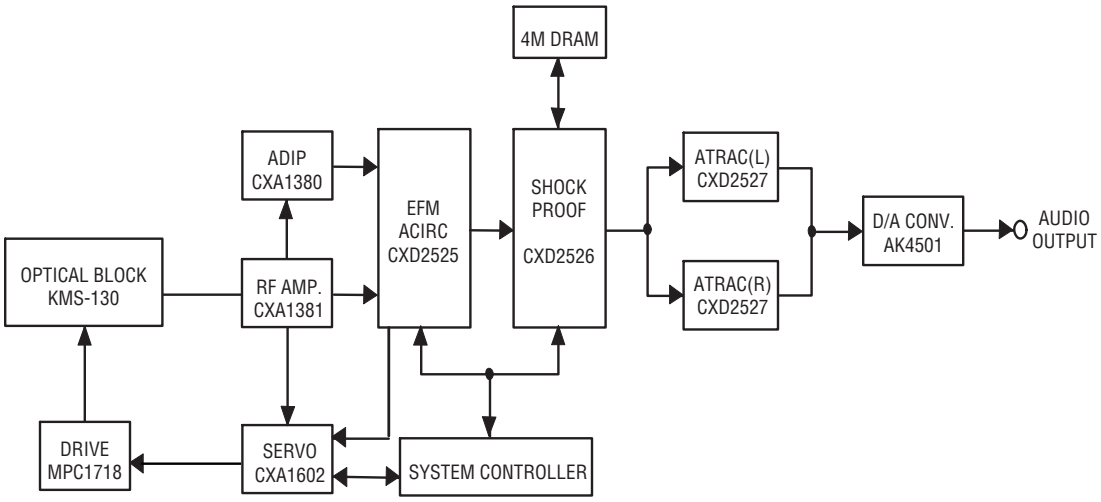


Fig. 3-1. First Generation Mini Disc System Block Diagram

(2) 2nd Generation [MZ-E2]

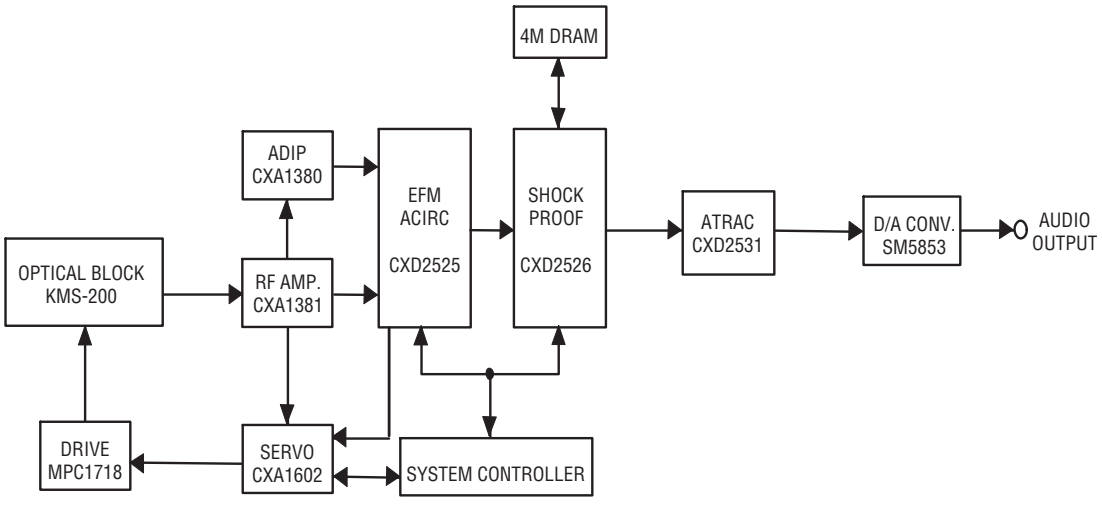


Fig. 3-2. 2nd Generation Mini Disc System Block Diagram

(3) 3rd Generation [MZ-E3/E40]

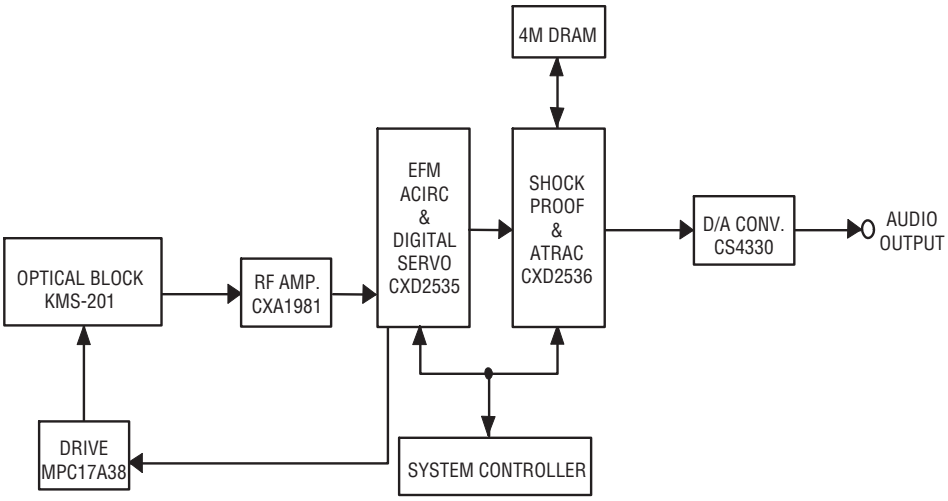


Fig. 3-3. 3rd Generation Mini Disc System Block Diagram

(4) 4th Generation [MZ-E30]

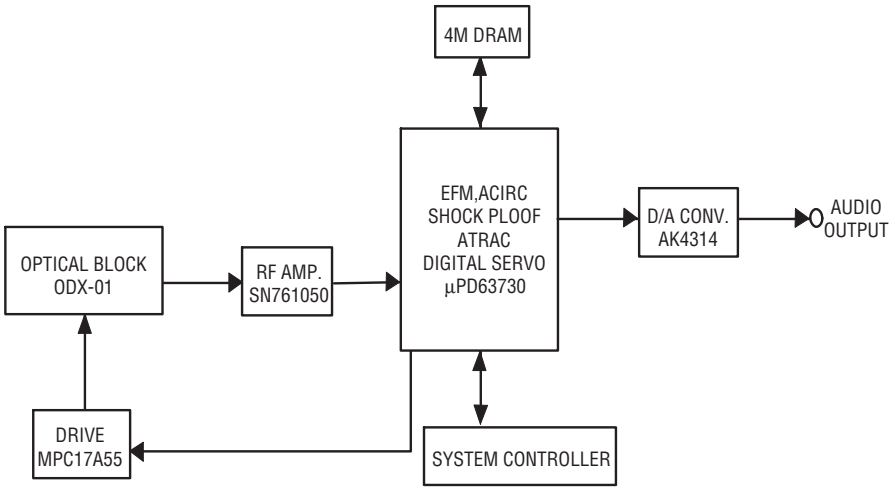


Fig. 3-4. 4th Generation Mini Disc System Block Diagram

4. OUTLINE OF SYSTEM

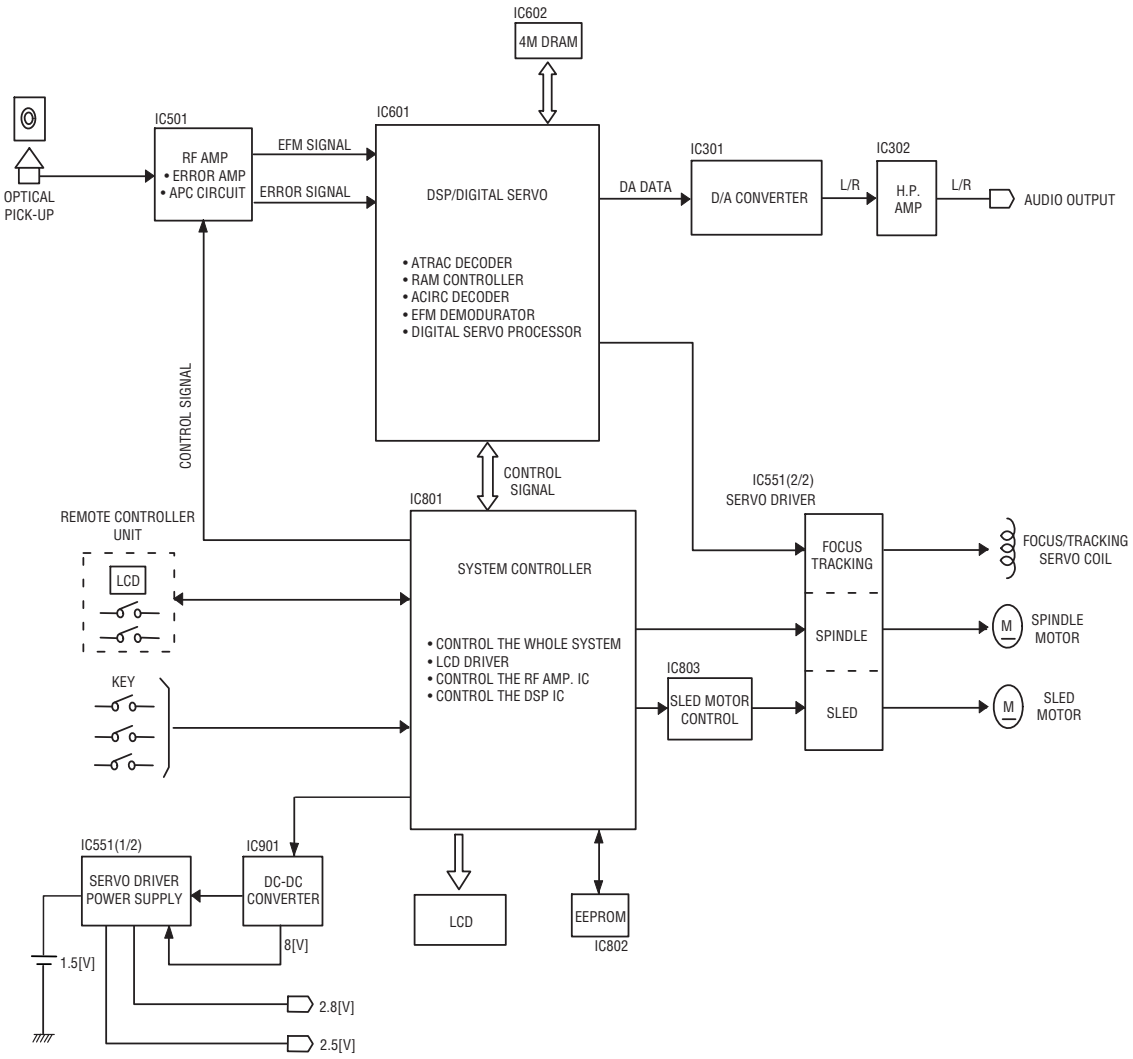


Fig. 4-1. General System Block Diagram

Fig. 4-1. is the general system block diagram. The MZ-E30 belonging to the fourth generation is generally composed of the system controller (IC801) to control the system as a whole as illustrated in the figure. In addition, a digital signal processor and a digital servo system are mainly composed of the DSP/digital servo LSI **µPD63730GC** (IC601) for playback.
Other main system components, moreover, include the servo driver (IC551) and RF amplifier (IC501), in which a power supply circuit is also included.

The DSP/digital servo **µPD63730GC** for playback is provided with most of those functions which are required for a Mini Disc to play back, such as ATRAC decoder, EFM decoder, ACIRC decoder, ADIP decoder, DRAM controller, etc. In addition, it comprises the digital servo (DSSP) and clock generator circuits. Built in the RF amplifier, moreover, are such circuits as the I-V converter amplifier capable of setting a gain, based on the serial data from the system controller, including a servo error extractor circuit, an APC circuit and so on.

The D/A converter (IC301) is of the low-voltage 1-bit type, in which a digital de-emphasize function is built, in addition to the digital filter applicable to 8-multiple oversampling and to a digital Dynamic Bass Boost (DBB). And the headphone amplifier (IC302) employed in the next stage is of low-power consumption type in which a mute function is incorporated.

The system controller serves to control the RF amplifier and the power supply circuit while processing a digital signal and controlling the digital servo, together with the DSP/digital servo. In addition, functions to detect a key-in and a remote control signal, and to control and drive the LCD are also available. The memory (IC802) connected to the system controller is an EEP ROM (nonvolatile memory) to store mainly servo-system data, such as a traverse supplementary value in the adjustment (overall regulation) mode, a focus bias, etc. Stored in this memory are the sound volume data just before the power supply enters the sleep mode, and the stop position address data to be used in the resume function. These data are transferred to each circuit upon startup.

4-1. Microprocessor Interface

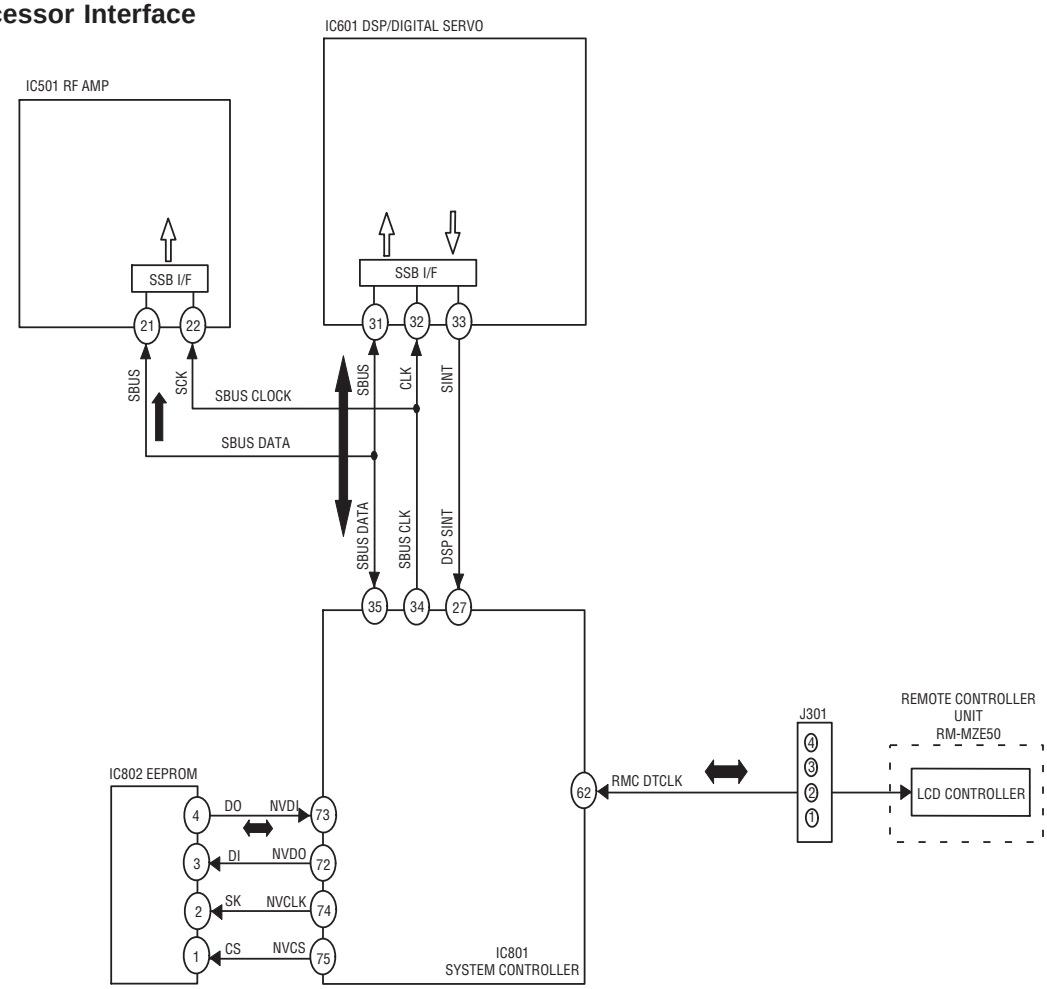


Fig. 4-2. Outline of Microprocessor Interface

The MZ-E30 has a microprocessor interface outlined in **Fig. 4-2.**. As shown in the figure, the system controller (IC801) is employed as the mainstay to control the system as a whole. Besides, the DSP/digital servo (IC601) and the EEP ROM (IC802) are provided. Commands and data are, moreover, bilaterally given and taken to and from the remote commander. In addition, data are unilaterally transmitted to the RF amplifier. Communications with the DSP/digital servo and RF amplifier, meanwhile, are performed by way of a serial bus (**SBUS**). Given and taken between system controller and DSP/digital servo mainly as described below, furthermore, are those serial data and serial commands which will be input and output to and from Pin ㉟ (SBUS DATA) as timed with the serial clock output from Pin ㉞ [SBUS CLK].

System Controller → DSP/digital servo (WRITE mode)
- Various function data in each digital servo (DSSP) and
- SERVO- and PLL-mode setting data, and electronic volume setting data

DSP/digital servo → System Controller (READ mode)
- Error data in each servo and
- SubQ/ADIP cluster and sector information

From the system controller to the RF amplifier, SBUS data are transferred similarly to the case of DSP/digital servo. And the clock line is used to set a gain in the I-V converter amplifier and ADIP extractor circuits located inside the RF amplifier, to adjust the balance of focus and tracking amplifiers, to amplify the RF, with pit or MO played back, and to select the servo amplifier polarity.

Between the system controller and the EEP ROM, a traverse supplementary value and a focus bias, both obtainable in the adjustment mode as already referred to, including such data as an offset value of focus/tracking gain, are transferred to and stored in the EEP ROM synchronously with the clock output from Pin ⑭ [NV CLK] of the system controller.
In the conventional model, moreover, the sound volume setting data and the address data relating to the stop position applied in the resume function are held in the RAM located in the interior of the system controller normally powered. In the MZ-E30, however, the power will stop being supplied to the system controller if the stop mode should last for about 10 second (which varies with an optical block position and/or with a mode) for the purpose of saving the energy. These data, therefore, are stored in the EEP ROM similarly to the servo system data so that they will be read out onto the system controller upon startup and transferred to each circuit.

Between the system controller and the remote commander, on the other hand, such display information as characters, etc. are transmitted by way of the remote jack (J301) to the LCD controller located inside the remote commander. Such information, moreover, is transmitted from the controller inside the remote commander to the system controller since the receiving data differ in transmission rate, etc. by type of remote control.
To transmit data, the clock timed with such data is also transmitted normally at a time. In the MZ-E30, however, clock information, etc. are previously transmitted, based on which the controller in the interior of remote control has a function of generating a clock. Only a single line for data, therefore, permits them to be received.

SBUS Data Transmission Timing

(1) Writing in DSP/digital servo or RF Amplifier from System Controller

To write in the DSP/digital servo or RF amplifier, each bit data are input synchronously with the falling edge of a serial clock (SCK) as shown in **Fig. 4-3.**. As shown in the figure, the first three bits relate to the control, with Bit 1 "**ST**" standing the for start bit, and Bit 2 "**R/W**" for the Read or Write mode.

Three types of information, command, address and data, are transferred from the system controller to the DSP/digital servo. To identify them, Bit 3 "**D/C**" should be used.

Commands and data, moreover, have a configuration as shown in **Fig. 4-4.**. When the code of a device coincides with that of a DSP/digital servo or of an RF amplifier, the device under the same code will receive the related command, thereby performing subsequent data communications. The instruction code, meanwhile, is used to transfer a command, such as to reset the hardware.

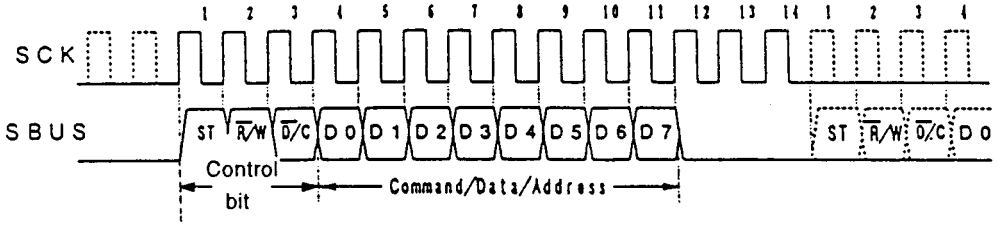


Fig. 4-3. Timing of Writing in DSP/digital servo or RF Amplifier from System Controller

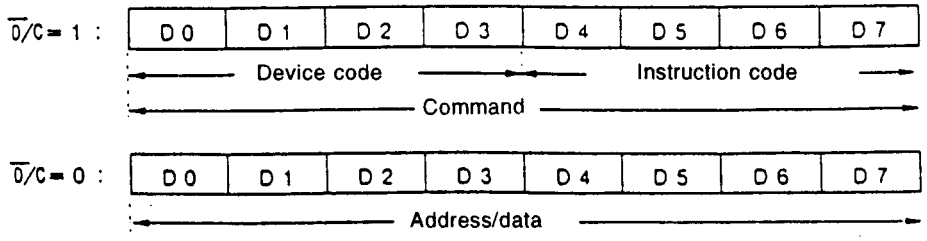


Fig. 4-4. Command and Data Configurations

(2) Reading onto System Controller from DSP/Digital Servo

To read from the DSP/digital servo, the information transferred to the system controller is limited to data only but free from Bit 3 "**D/C**" as shown in **Fig. 4-5.**. The DSP/digital servo has an SBUS terminal employed as an output port only during the bit period for which data are being output. In any other section, the DSP/digital servo has high impedance.

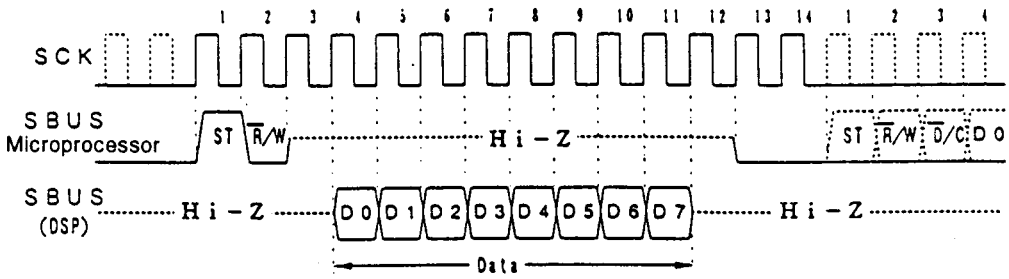


Fig. 4-5. Timing of Reading onto System Controller from DSP/digital servo

4-2. Clock System

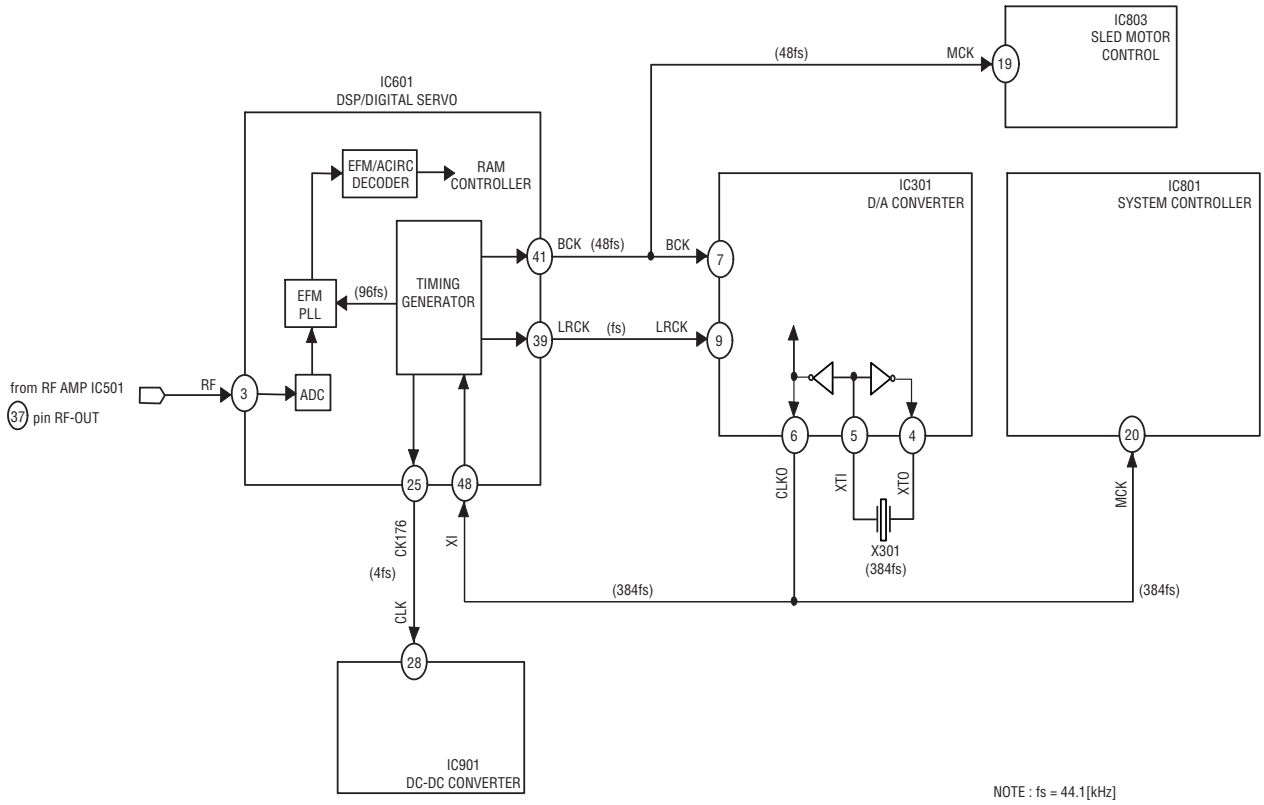


Fig. 4-6. Clock System Block Diagram

Fig. 4-6. shows a block diagram of the clock system.

For the master clock of both system controller (IC801) and DSP/digital servo (IC601), 384 fs (fs = 44.1kHz) available at X301 connected between Pin ⑤ [XT1] and Pin ④ [XT0] in the D/A converter (IC301) is supplied from Pin ⑥ [CLK0].

The timing generator located in the interior of the DSP/digital servo divides a frequency of 384 fs input at Pin ㊽ [X1] so as to output 48 fs (bit clock) from Pin ㊶ [BCK], fs (L/R clock) from Pin ㊴ [LRCK] and 4 fs from Pin ㉕ [CK176].

Based on a frequency of 96 fs from the timing generator, the EFM PLL unit generates a PLL clock (PLCK) so as to perform EFM demodulation in a subsequent stage of the EFM decoder.

A frequency of 48 fs (bit clock) supplied to Pin ⑲ [MCK] in the sled motor control (IC803) is used as the master clock for the controller located inside. And the bit clock (BCK) and L/R clock (LRCK), both output to the D/A converter, are used as the timing signal for the audio data output from the ATRAC block in the DSP/digital servo. (For details, refer to **7-2. Playback Operations.**)

A frequency of 4 fs, which is output from Pin ㉕ [CK176] in the DSP/digital servo to Pin ㉘ [CLK] in the DC-DC converter is used as a switching signal to drive the STEP-UP circuit in the power supply unit. (For details, refer to **5-1. Outline of Power supply Circuit Operations.**)

5. POWER SUPPLY CIRCUIT

Fig. 5-1. shows an outline of the power supply circuit employed in the MZ-E30, as shown in the figure, the power supply voltages applied to the MZ-E30 may be divided, if roughly classified, into three: 1.5V, 2.8V and 2.5V lines. 2.8V (VC) is obtained by raising the 1.5V voltage in the step up circuit (2) and supplied to principal circuits, such as D/A converter (IC301), including system controller (IC801) and DSP/digital servo (IC601).
A voltage of 8V obtained in the step up circuit (1) and in the charge pump circuit, moreover, is supplied to the servo driver (IC551) and 2.5V to the RF amplifier (IC501) and to the optical block.

To save the electric power, the MZ-E30 has the step up circuits stop operating according to the sleep signal which the system controller will output if the STOP mode should last for about 10 seconds (which varies with an optical block position and/or with a mode). As a result, the power will also stop being supplied to each component. To startup, on the other hand, a wakeup circuit will start up when a operation button located in the remote commander or in the unit is pressed. This will cause the step up circuit to start operating so that the power is supplied to each component. In addition, this power-saving feature also interlocks with the ON/OFF operations of the disc door opening/closing detector switch. The power supply then enters the wakeup (startup) or sleep (standby) mode immediately.

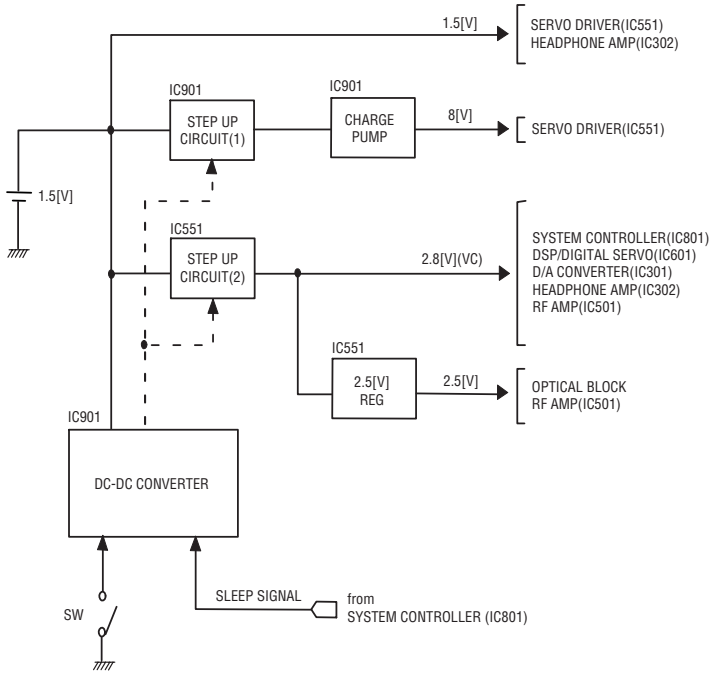


Fig. 5-1. Outline of Power Supply Circuit

5-1. Outline of Power supply Circuit Operation

Fig. 5-2. shows the power supply circuit block diagram and timing of waveforms in wakeup (startup) and sleep (standby) modes.

Operating a key on the unit or in the remote commander connected to Pin ㉟ [XWK1] thru Pin ㉜ [XWK4] in the DC-DC converter (IC901) will cause the related input pin to become "L," thereby causing the system control (wakeup/sleep control) circuit inside to start up.

This will also cause the internal oscillator (OSC1) in the same IC, the step up circuit (1), and the charge pump circuit to start operating. Subsequently, the internal

oscillator (OSC2) will also begin to operate. As a result, a switching PWM wave of about 200 kHz is output from Pin ㉒ [PWM1], and a switching power control mode signal from Pin ㉑ [DI]. This will cause the step up circuit (2) inside the servo driver (IC551) to start operating. In addition, the power switch (connected between Pins ④, ⑤ and ②, ③) will also turn on. Thus, 2.8V (VC) will be supplied to each component.

At the same time, a voltage of 2.5V output from the 2.5V REG circuit in the interior is supplied from Pin ㊹ [VREG] to the optical block and to the RF amplifier (IC501).

With 2.8V (VC) applied to Pin [10] [VC] in the DC-DC converter, a RESET signal ❻ is sent from Pin ⑧ [XRST], thereby causing each IC to start operating. The frequency of 176 kHz (4 fs : fs = 44.1 kHz) obtained, with a frequency of 384 fs available at X301 divided by 96, enters Pin ㉘ [CLK] from the DSP/digital servo (IC601). Thus, a switching operation continues so that the step up circuits (1) and (2) will have their respective Drives OSC1 and OSC2 switched over to an external clock (4 fs).

If the voltage of 2.8V (VC) fluctuates, the saw-toothed generator (SAW) inside the DC-DC converter compares the saw-toothed wave obtained from the external clock (4 fs) with the VC input in Pin ⑩. The generator will control the duty ratio of a PWM wave output from Pin ㉒, thereby controlling 2.8V (VC).

The latch clear signal ❼, which is input from Pin ⑱ [XWK CLR] in the system controller to Pin ㉛ [FF CLR] in the DC-DC converter, will have "L" input in either one of XWK1 thru 4 according to an FF (flip-flop) RESET signal inside the system control in the DC-DC converter. All other input circuits are prohibited from being set until the latch clear signal has become "H" after setting the FF.

To switch over to the sleep mode, on the other hand, the sleep signal ❽ is output from Pin ⑲ [SLEEP] in the system controller once the STOP mode has lasted for about 10 seconds (which vary with the optical block position and/or with a mode) or immediately after the door has opened. This will cause the step up circuits (1) and (2) to stop operating while ceasing to supply the power to each component.

5-2. Operation in Wakeup (Startup) Mode

In the sleep mode, when the following operations are performed, the system control (Wakeup/Sleep control) circuit inside the DC-DC converter starts up. Each power supply circuit starts operating to supply power supply voltage to each component.

- Press the operation button on the unit.
- Press the operation button in the remote commander.
- Close the disc door.

Once a button operation has been performed either on the unit or on the remote commander, the MZ-E30 will enter such a mode as shown in **Table 5-1.** after waking up. Once the open/close switch (S801) has turned on with the disc door closed, moreover, the MZ-E30 will switch over to the STOP mode after waking up.

Table 5-1. Operations upon Wakeup with Operation Switch

Operation Button	Operation on the Body	Operation by Remote Commander
PLAY	O	O
STOP	Δ	Δ
FF	○	Also used as PLAY button
REW	○	O
PAUSE	—	Δ
VOL +	○	○
VOL −	○	○
PLAY MODE	○	○
DISPLAY	—	Δ

O: Post-wakeup PLAY Mode
○: Post-wakeup STOP Mode (with disc rotating for several seconds)
Δ: Waking up but no indication on LCD
—: None

(1) Wakeup by Operating Buttons on the Unit

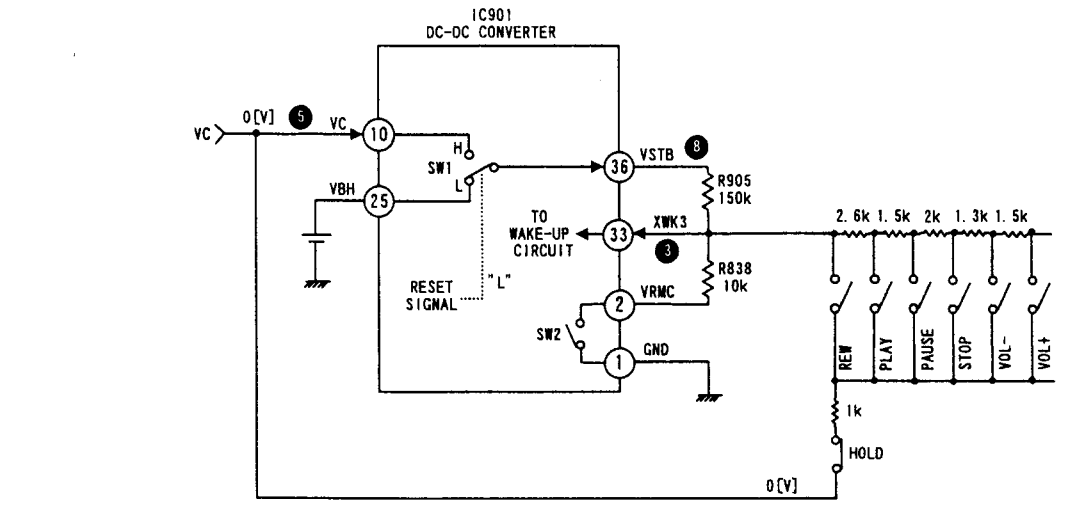
Fig. 5-3. shows a wakeup circuit. In the sleep mode, the power supply circuit has stopped operating. The DC-DC converter (IC901) is therefore 0V at Pin ⑩ [VC]. SW1, which performs switching according to the RESET signal in the DC-DC converter is therefore connected to Pin ㉕ [VBH] and a voltage (about 1.5V) at both ends of the battery is output from Pin ㊱ [VSTB]. If the PLAY button is then pressed on the unit, Pin ㉜ [XWK4] becomes "L", thereby causing both wakeup and power supply circuits to start up so as to supply each power supply voltage to each component. Subsequently, the RESET signal becomes "H" and SW1 inside the DC-DC converter is connected to Pin ⑩ so that 2.8V (VC) is output from Pin ㊱. With the PLAY button turned on, moreover, Pin ⑤ [PLAY KEY] will also become "L" in the system controller (IC801). Consequently, the MZ-E30 will switch over to the PLAY mode as shown in **Table 5-1.** after waking up.

Pressing any button other than the PLAY, on the other hand, will cause Pin ㉟ [XWK1] to become "L" so that the MZ-E30 will perform a wakeup operation, likewise. A divided voltage, moreover, is input to Pin ⑧ [SET KEY] in the system controller after a voltage of 2.8V (VC) output from Pin ㊱ in the DC-DC converter has been divided by R808 (47 kΩ) and a matrix resistance. Based on its potential, the MZ-E30 determines the mode and switches over mainly to the STOP mode as shown in **Table 5-1.**.

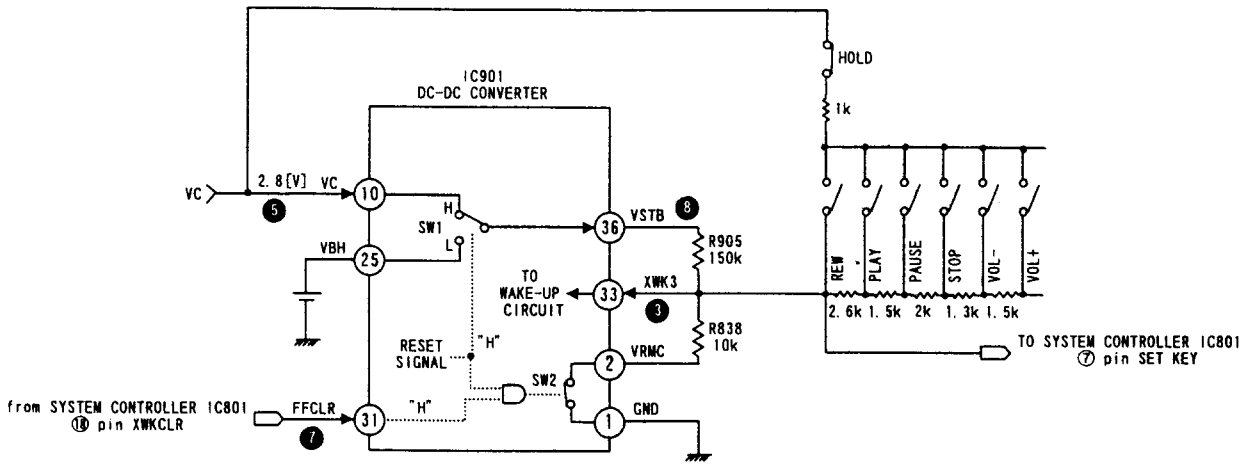
Only the PLAY button is connected to the wakeup circuit and to the system controller to prevent the MZ-E30 from malfunctioning. This ensures that the MZ-E30 will not fail to enter the related mode even if the PLAY button is pressed instantaneously.

(2) Wakeup by Operating Buttons in Remote Commander

In the sleep mode, SW2 in the DC-DC converter (IC901) has turned off as shown in **Fig. 5-4 (a).**. As a result, the voltage (approx. 1.5V)) at both ends of the battery, which is output at Pin ㊱ [VSTB], is applied to Pin ㉝ [XWK3] via pull-up resistor R905 (150 kΩ). Besides, each power supply circuit has stopped operating. As a result, Pin ⑩ [VC] becomes 0V. In this stage, operating any remote commander button will cause Pin ㉝ to become "L" since the matrix resistance inside the remote commander is small enough for R905. Consequently, the wakeup and power supply circuits will start up, thereby supplying components with their respective power supply voltages. SW1, furthermore, is positioned at Pin ⑩ synchronously with a RESET signal. SW2, moreover, turns on synchronously with the latch clear signal to be input from the system controller to Pin ㉛ [FFCLR]. Pin ② [VRMC] is connected to GND as shown in **Fig. 5-4 (b).**. Thus, 2.8V (VC) is output from Pin ㊱. Pin ⑦ [RMC KEY] in the system controller will receive two inputs: one is a parallel resistance value dependent upon the matrix resistance of R905 and in the remote commander, and the other is a divided voltage obtained at R838 (10 kΩ). This allows the MZ-E30 to determine the mode so as to switch over to the mode shown in **Table 5-1.**.



(a) In the Sleep Mode



(b) In the Wakeup Mode

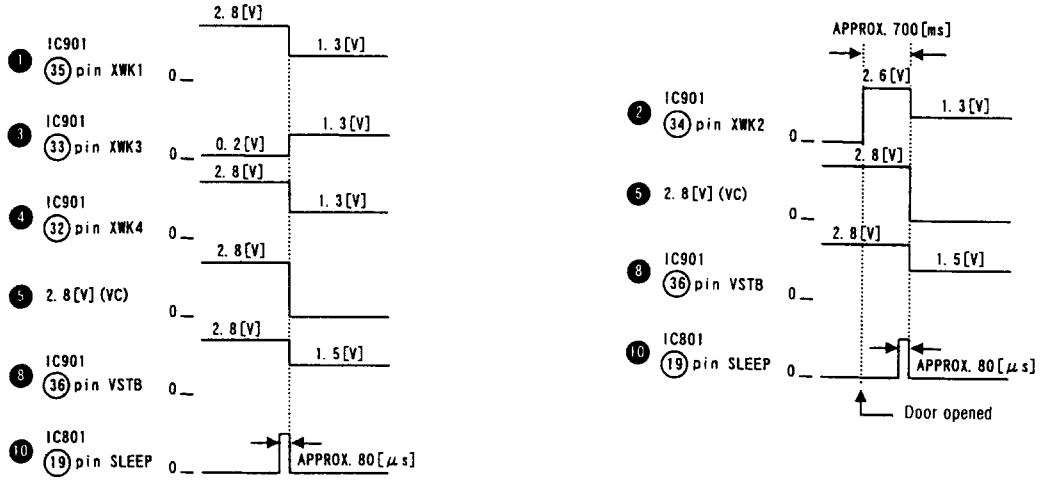
Fig. 5-4. Wakeup Operation by Operating Buttons in Remote Commander

(3) Wakeup with Disc Door Closed (Refer to Fig. 5-3.)

When the disc door is opened for such a purpose as to replace the disc or the like, the open/close switch (S801) has turned off. To immediately switch over to the sleep mode, a voltage (about 1.5V) at both ends of the battery will be output from Pin ㊱ [VSTB] in the DC-DC converter. This voltage is applied to Pin ㉞ [XWK2] via pull-up resistor R804 (47 kΩ).
With the disc door closed, the open/close switch turns on, thereby causing Pin ㉞ to become "L." Both wakeup and power supply circuits will start operating so that components will be supplied with their respective power supply voltages. (Refer to waveform ❷ as illustrated in **Fig. 5-3.**.)
In the system controller, moreover, Pin ⑥ [OPN/CLS SW] will also become "L." After waking up as already referred to, the MZ-E30 will change over to the STOP mode.

5-3. Operation in the Sleep (Standby) Mode (Refer to Fig. 5-3.)

Fig. 5-5. shows the timings of waveforms in the sleep mode. If the STOP mode (with the disc rotating) should last for 10 seconds (which vary with an optical block position and/or with a mode), the MZ-E30 will first of all move to the TOC position in the optical block. At the same time, the sound volume data and the address data at the stop position to be used in the resume function are transferred to the EEP ROM (IC802). Immediately, an about 80 μs sleep signal is output from Pin ⑲ [SLEEP] in the system controller (IC801) in such timing as shown in **Fig. 5-5. (a)** ❿. As a result, the FF (flip-flop) in the DC-DC converter will be reset. This will cause the respective power supply circuits to stop operating while 2.8V (VC) changes over to 0V. SW1 in the DC-DC converter is connected to Pin ㉕ [VBH] and a voltage (about 1.5V) at both ends of the battery will be output from Pin ㊱ [VSTB]. All the Wakeup Inputs Pins ㉟, ㉝ and ㉜ [XWK1, 3 and 4] will change over to about 1.3V.
If the disc door should be opened in the wakeup mode, on the other hand, a sleep signal will be output after approx. 700 ms (which vary with an optical block position) as shown in **Fig. 5-5. (b)** ❷. The MZ-E30 then switches over to the sleep mode. For this duration of approx. 700 ms, the optical block is, likewise, moved to the TOC position and the sound volume data will be transferred to the EEP ROM.



(a) When STOP Mode Lasts about 10 Seconds **(b) When Disc Door is Opened**

Fig. 5-5. Timings of Waveforms in Sleep Mode

5-4. Detecting Decrease in Voltage

Fig. 5-6. shows a block diagram of the battery voltage monitor circuit. When Pin ㉖ [UREG CHK CON] in the system controller becomes to "H," the VOLT CHECK (Q801) turns on. This will cause the voltage at both ends of the battery to be divided or halved in the R801 and R802. And the voltage so halved is input to Pin ② [UREG MON] in the system controller, thereby detecting a decrease in voltage. A battery voltage of 0.8V or less will cause the MZ-E30 to be put into the STOP mode, with Message "LoBATT" blinking on the remote commander display. In approximately 5 seconds, a sleep signal will be output from Pin ⑲ [SLEEP] in the system controller so that the power supply circuit will stop operating. Upon wakeup, meanwhile, Pin ㉖ in the system controller will change from "L" to "H" at the timing shown.

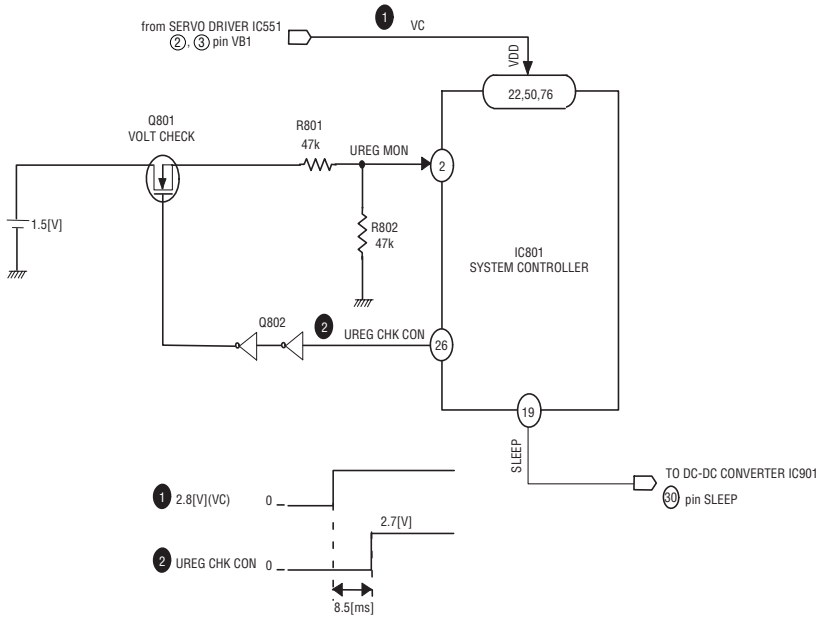


Fig. 5-6. Battery Voltage Monitor Circuit

5-5. RESET Circuit

Fig. 5-7. shows the RESET circuit and the RESET signal timing. The 2.8V (VC) obtained in the step up power supply circuit of the motor driver (IC551) enters the RESET circuit after being divided with a resistor inside via Pin ⑩ [VC] in the DC-DC converter (IC901). In the RESET circuit, the capacitor connected to Pin ⑦ [CRST] outputs the RESET signal from Pin ⑧ [XRST] to main ICs, such as system controller (IC801) and DSP/digital servo (IC601), at the delayed timing shown in the figure.

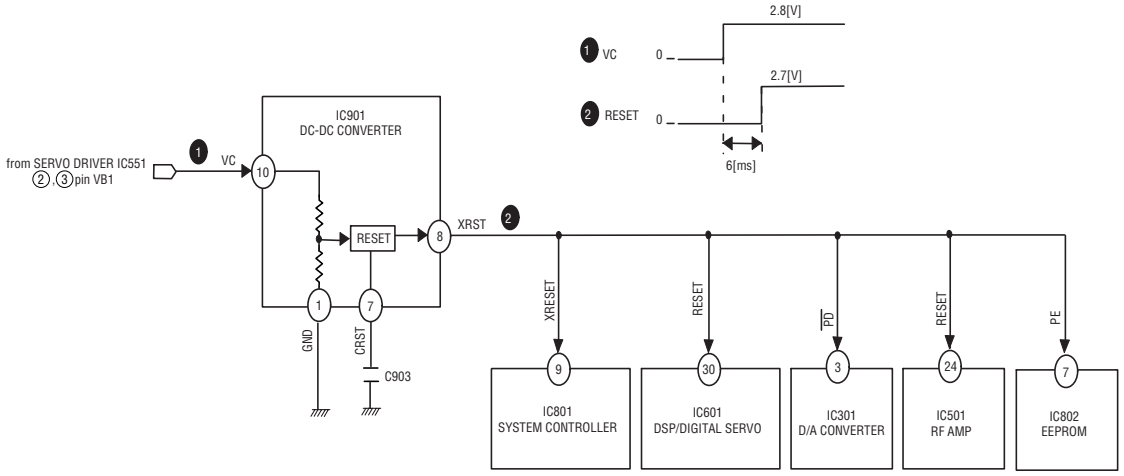
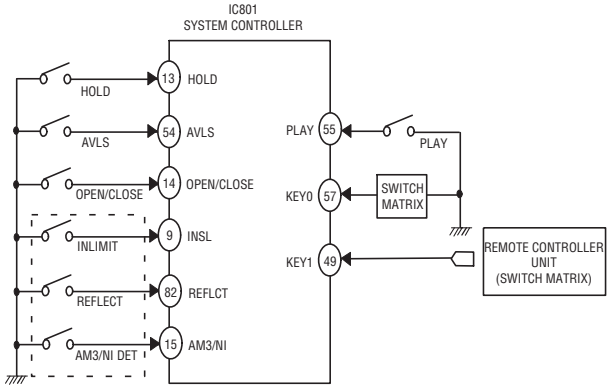


Fig. 5-7. RESET Circuit and RESET Signal Timing

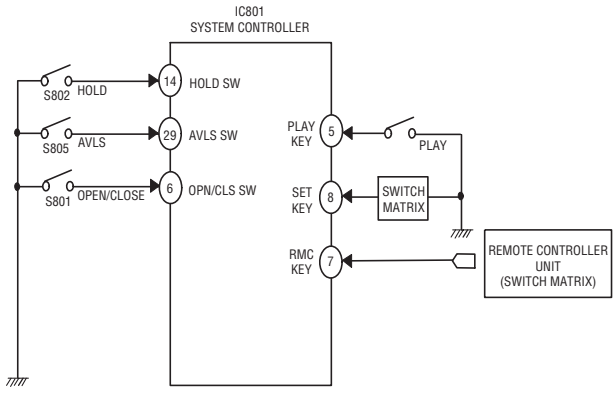
6. SYSTEM CONTROL

6-1. Detection Switch

Fig. 6-1. shows the detection switches connected to the system controller (IC801) and switch matrix for differentiating the mode. This unit comes without the part enclosed in the dotted lines in **(a) of the same figure** which were provided with the 3rd generation unit, namely LIMITIN (detects the innermost circumference of the optical block), REFLECT (detects the reflectivity rate of the disc), and the switches for differentiating and detecting the battery. Due to the omission of these parts, focus search after disc replacement, etc. is performed at other than the innermost circumference in this unit. When the servo turns ON, and data can be read from the disc, TOC accessing is performed based on the address.
Moreover, the differentiation of the MO or playback only disc which was performed by the reflectance rate detection switch is performed in this unit by alternately switching the internal gain and laser power settings of the RF amplifier during focus search, and detecting at which of these settings the focus turns ON.
(Details of differentiation of the disc are provided in **8-3. Focus Search and Disc Differentiation.**)
As this unit uses a single voltage and does not have a recharge function, it is not mounted with a switch for differentiating and detecting the battery.
At the ON and OFF of the open/close switch (S801), the wakeup (startup) and sleep (standby) operations of the power supply are controlled, and at the same time, clearing of the address data of the stop position used by the resume function is performed.



(a) Example of MZ-E3



(b) MZ-E30

Fig. 6-1. Detection Switch Connected to System Controller

6-2. Key Input Detection of Operation Buttons

The operation buttons on the unit and remote commander are each composed of switch matrix by combining with the dividing resistor. As shown in **Fig. 6-1. (b)**, when a operation button on the unit or a operation button on the remote control unit is pressed, the voltage corresponding to the mode determined by the dividing resistor is input to Pin ⑧ [SET KEY] or Pin ⑦ [REM KEY] of the system controller (IC801) respectively. The system controller differentiates the mode according to this input voltage, and sets the corresponding mode. As no power is supplied to the system controller in the sleep (standby) mode, it will differentiate the mode after a button is pressed and power is supplied.

(1) When operating using the unit

Fig. 6-2. shows the connection between the operation buttons on the unit and the system controller (IC801) while **Table 6-1.** shows the voltage input to the key input Pin ⑧ [SET KEY] of the system controller when a operation button is pressed.

When power supply to each part starts after wake-up, 2.8V (VC) from Pin ㊱ [VSTB] is supplied to R808 (47 kΩ) via the switch inside the DC-DC converter (IC901). When a operation button is pressed in this state, a dividing voltage determined by R808 (47 kΩ) and the resistor corresponding to that operation button, is input to Pin ⑧ of the system controller. A separate line from the switch matrix is incorporated only for the PLAY button and voltage is input separately to Pin ⑤ [PLAY KEY] so that the PLAY mode is set even when the button has been pressed instantaneously.

Table 6-1. Key Input Voltage During Operations of Unit (Reference Values)

Operation Buttons of Unit	Pin ⑧ of IC801
STOP	0V
FF	0.15V
REW	0.4V
VOL +	0.6V
VOL –	1.0V
P-MODE	1.5V
When nothing is pressed	2.8V

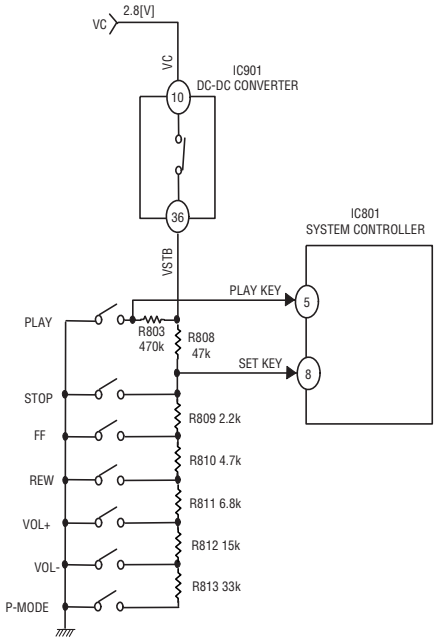


Fig. 6-2 Key Input Circuit of Operation Buttons of Unit

(2) When operating using the remote commander

Fig. 6-3. shows the connection between the operation buttons on the remote commander and the system controller (IC801) while **Table 6-2.** shows the dividing voltage input to Pin ⑦ [RMC KEY] of the system controller when a remote commander button is pressed.

When power supply to each part starts after wake-up, the two switches inside the DC-DC converter turn ON, and the dividing voltage obtained by R905 (150 kΩ) and R838 (10 kΩ) is input to Pin ⑦ [RMC KEY] of the system controller. When a remote commander button is pressed in this state, the matrix resistor corresponding to that button and a dividing voltage and R905 are connected in parallel form, and the voltage shown in **Table 6-2.** is input to Pin ⑦ of the system controller.

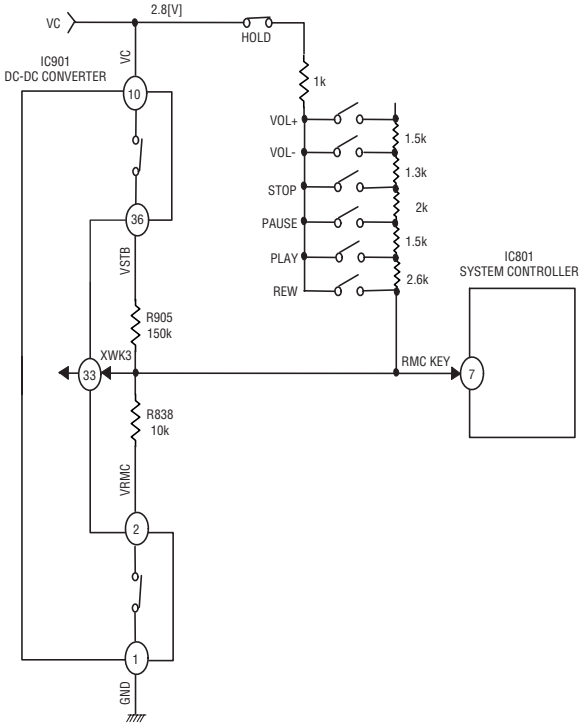


Fig. 6-3. Key Input Circuit of Remote Commander

Table 6-2. Key Input Voltage During Operations of Remote Commander (Reference Values)

Operation Buttons of Remote Commander	Pin ⑦ of IC801
VOL+	1.4V
VOL–	1.5V
STOP	1.65V
PAUSE	1.8V
PLAY (FF)	2.0V
REW	2.5V
When nothing is pressed	0.2V

6-3. operation of APC Circuit and Laser Power

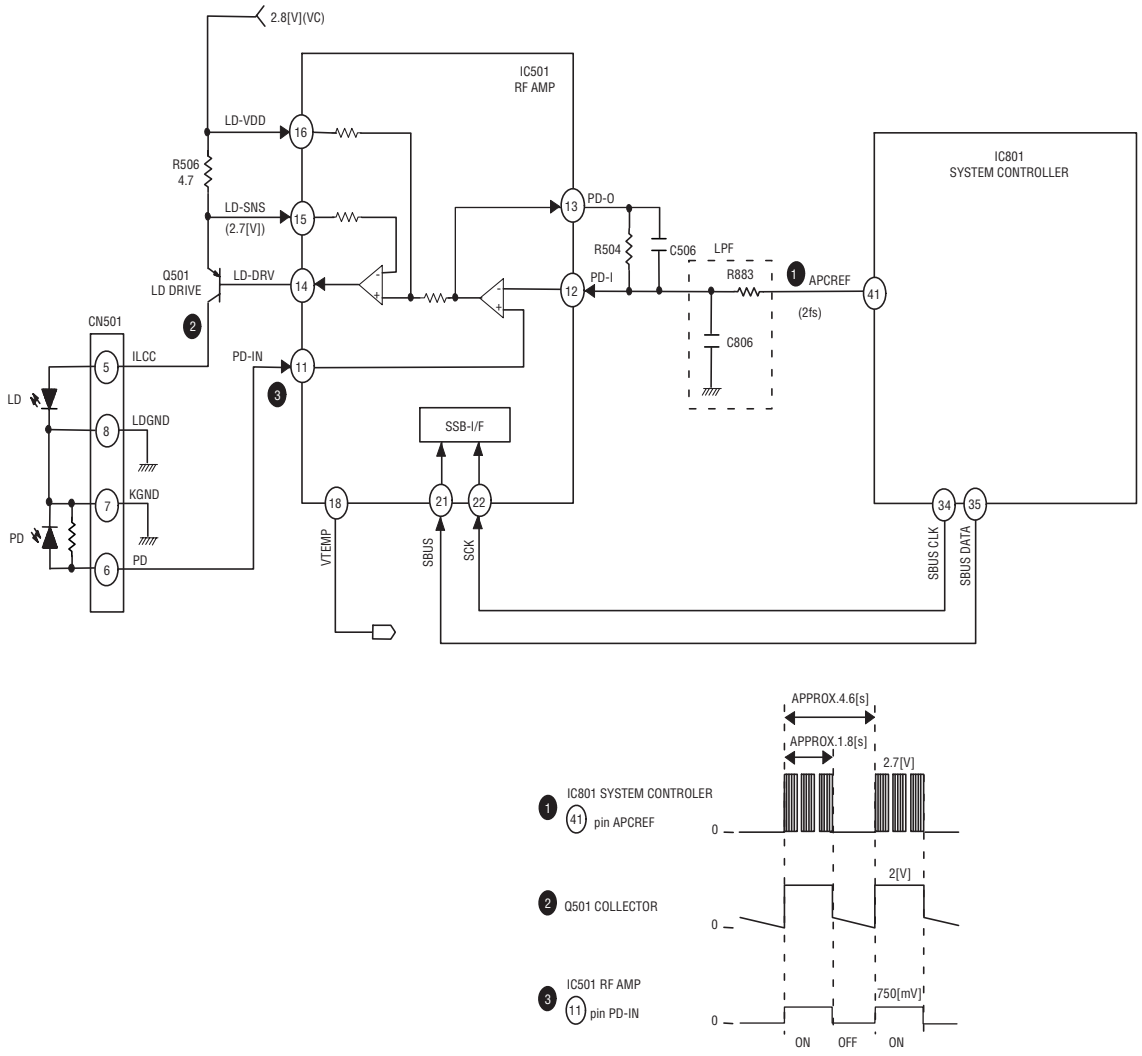


Fig. 6-4. APC Circuit and Waveform Timing

Fig. 6-4. shows the APC (Automatic LASER Power operation) circuit and main waveform timings. The APC circuit controls the driving current of the laser so that the voltage supplied from outside becomes the same as the monitor diode voltage. With functions such as PLAY where the laser diode emits light, Pin ㊶ [APC REF] of the system controller (IC801) outputs a 88.1 kHz (2 fs:fs=44.1 kHz) PWM waveform at the waveform timing (❶) shown in the figure. In the LPF, the DC APC REF signal is input to Pin ⑫ [PD-I] of the RF amplifier (IC501), passed through the two differential amplifiers inside, output from Pin ⑭ [LD-DRV], passed through the LD drive (Q501) to drive the laser diode inside the optical block.

Inside the monitor diode (PD), the photoelectric current corresponding to the amount of radiated laser light is converted to voltage by the resistor connected between the monitor diode anode and GND, input to Pin ⑪ [PD-IN], and fed back to the first stage amplifier to control the laser power. A constant current circuit is composed by feeding back the voltage decreased by the R506 resistor (4.7 Ω) connected to the emitter of the LD drive, so that the driving current does not change even when the power supply voltage changes.

The ON/OFF of the laser driving current is controlled by the system controller via the serial bus (SBUS).

During normal playback, an approximately 1.8 seconds ON and 2.8 seconds OFF are repeated as shown by the timing in the figure to save power.

In models which can record, changes in the recording power of the disc according to the ambient temperature and internal temperature of the unit are detected by the temperature sensor and compensated. The RF amplifier (IC501) has a function which converts temperature into voltage and outputs it from Pin ⑱ (VTEMP), but this function is not used in this unit intended exclusively for playback.

As the optimum read power differs between the playback only disc and MO disc, the disc is differentiated by focus search performed immediately after the unit is started. The duty ratio of the PWM wave output from Pin ㊶ of the system controller is controlled so that 0.6 mW power is obtained if the disc is a playback only disc, and 0.8 mW power is obtained if it is a MO disc.

(Details of differentiation of disc are provided in **8-3. Focus Search and Disc Differentiation.**)

7. PLAYBACK CIRCUIT

7-1. Outline of Playback Circuit

Fig. 7-1. shows the structure of the playback circuit of the Mini Disc. The RF data read by the optical block is demodulated by the EFM demodulator, and data errors are detected and corrected by the ACIRC decoder.

Since the Mini Disc data has the same structure as the CD-ROM, it is decoded in the CD-ROM decoder in the next step, and the ATRAC data compressed to approximately 1/5 is stored in the shock proof memory (buffer RAM). Apart from the ATRAC data, this memory also stores error information (C2PO) and TOC/UTOC information.

The ATRAC data is written in the memory intermittently, and read to the ATRAC decoder periodically. The compressed data is expanded to 16-bit linear data by the ATRAC decoder, D/A converted by the D/A converter, and output as analog signal.

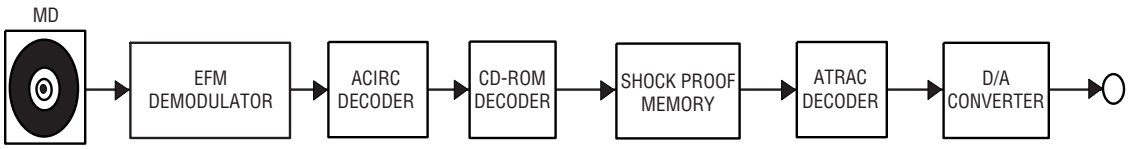


Fig. 7-1 Structure of Mini Disc (Playback Circuit)

7-2. Playback Operations

Fig. 7-2. shows the block diagram of the playback circuit and the waveform of the main parts.

The two RF signals (I and J signals) I-V converted inside the optical block are input respectively to Pins ⑥ (VI) and ⑦ (VJ) of the RF amplifier (IC501). The RF amplifier sets the gain and internal circuits according to the disc type (MO or CD) using the serial data input form the system controller (IC801).

Disc discrimination and gain setting are performed together during focus search. (Details are provided in **8-3. Focus Search and Disc Discrimination.**)

Furthermore, the output of the RF amplifier (1) is switched according to the disc type written in the TOC. In the case of the pit area of the playback only disc and MO disc, the additional signal of I and J is output, based on the Vref voltage (0.88V) generated inside the RF amplifier, from Pin ㊲ (RF-OUT) to the DSP/digital servo (IC601) via the RF amplifier (2) and EQ (equalizer). In the case of the groove area (UTOC, program area) of the MO disc, the subtraction signal is output. (❶)

The RF signal is converted to a 7-bit digital value at a sampling frequency of 4.23 MHz (96 fs:fs=44.1 kHz) by the A/D converter inside the DSP/digital servo. In the EFM PLL circuit, clock extraction and generation are performed, and based on the channel clock (4.23 MHz) obtained, EFM demodulation is performed in the next stage. In the ACIRC decoder, data errors are detected and corrected, and the data is then written in the DRAM via the RAM controller. The accumulated data is compressed to approximately 1/5 according to the transfer command from the system controller, and periodically sent to the ATRAC decoder block. In the ATRAC decoder block, the compressed data is expanded, and the data is output continuously to the D/A converter (IC301) from Rch and Lch alternately in synchronization with LRCK (L/R clock) and BCK (bit clock) at the timing of the audio signal shown in the figure.(**Refer to ❷ to ❹.**)

The D/A converter is also incorporated with a digital DBB (Dynamic Bass Boost) and eight times over sampling digital filter. These perform boosting of low bands and data filtering respectively using digital signals. The D/A converter also has a deemphasis function, which is controlled using the emphasis ON and OFF signals output from Pin ㊳ (EMP) of the DSP/digital servo. The D/A converted analog signal is output to the headphone amplifier (IC302) via the VOLUME DOWN circuit (Q301), which attenuates the audio signal boosted when DBB is ON, from Pins ⑰ and ⑯ (A OUT L, AOUT R).

When the VOL button connected to the system controller is operated to control volume, the volume data is sent to the ATRAC decoder block of the DSP/digital servo (IC601) via the serial bus (SBUS) and the volume is controlled by digital signal processing inside the block.
Likewise for the beep sound when the remote operation button is operated, the data is sent to the DSP/digital servo (IC601), the beep signal is generated inside the DSP/digital servo and output to the headphone via the D/A converter and headphone amplifier.

7-3. Digital DBB and Mute Circuit

Fig. 7-3. shows the digital DBB (Dynamic Bass Boost) and mute circuit.

The D/A converter (IC301) incorporates a digital DBB function which is switched ON/OFF using the DBB switch (S301) connected to Pin ⑪ (DBB0) and Pin ⑫ (DBB1).
Low bands are boosted using the digital signal.
When Pin ⑪ is set to "H", at the reference level (–12 dB), signal is boosted by about 3.5 dB for 100 Hz. When Pin ⑫ is set to "H", it is boosted by about 8.5 dB. When DBB is turned ON, Q301 connected between the D/A converter and headphone amplifier (IC301) also is turned ON at the same time. As a result, R206 (15 kΩ) and R202 (6.8 kΩ) or R106 and R102 are connected in parallel, and attenuate the volume boosted by the DBB to prevent clipping caused by the volume increasing and excess input to headphone amplifier when the DBB is ON.

On the other hand, the headphone standby signal from Pin ⑦⓪ (HP STBY) or the mute signal from Pin ⑥⑨ (HP MUTE) of the system controller is input to the headphone amplifier to turn the standby mode and mute. When the standby signal is set to "H" or the mute signal is set to "L" as shown in the timing chart in the figure, the sound signal input from the D/A converter is output from the headphone.
During wakeup, and immediately after the PLAY mode is set, the headphone is muted by the approximately 500 to 600 ms mute signal output from the system controller to prevent the output of pop noise, etc.

8. SERVO CIRCUIT

8-1. Outline of Servo Circuit

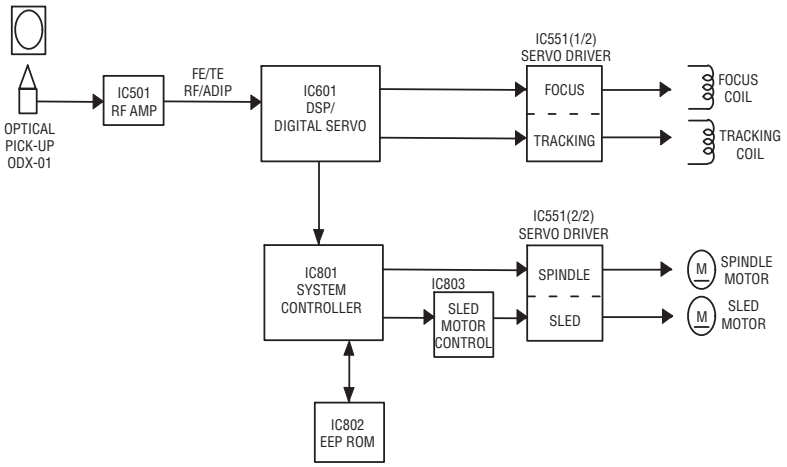


Fig. 8-1 Outline of Servo Circuit

As shown in **Fig. 8-1.**, the servo circuit is composed of the RF amplifier (IC501), DSP/digital servo (IC601), system controller (IC801), and the servo driver (IC551).

When a playback disc is played, the servo circuit operates in the same way as the CD player.

The focus and tracking servos A/D convert the error signals output from the RF amplifier inside the DSP/digital servo (IC601), and perform servo calculation and correction. They then convert the signals to 2 fs (fs=44.1 kHz) PWM wave and output them to drive the focus and tracking coil using the servo driver (IC551).

The spindle servo sends the measured period of the EFM frequency divided signal obtained from the RF signal using the DSP/digital servo (IC601) to the system controller, generates the spindle error signal inside, and controls the rotation of the spindle motor via the servo driver. The sled servo A/D converts the tracking error signal, sends the data to the system controller, and generates the control signal of the sled motor control (IC803). The sled error signal is generated from this control signal in the sled motor control (IC803) in the next stage, and used to control the rotation of the sled motor via the servo driver.

When the MO disc is played back, only the spindle servo in the servo circuit differs from when the playback only disc is played back. In the case of the playback of the playback only disc, the measured period of the EFM frequency divided signal obtained from the RF signal is used. In the case of the MO disc, that of the frequency divided signal obtained from the ADIP signal recorded in the groove area is used.

In this unit, the digital servo composed of the RF amplifier (IC501), DSP/digital servo (IC601), and system controller (IC801) controls focus, tracking, sled, and spindle. RF level adjustment and ABCD level adjustment are performed automatically immediately after the unit is started by pressing the PLAY button so that the optimum values according to the disc type (CD/MO) can be obtained by the digital servo.

The adjustment values of the servo such as focus/tracking gain, EF balance, focus bias, etc. stored in the non-volatile memory (IC802, EEPROM) are sent to the servo circuit when the adjustment mode is started to optimize the servo. (Details of the adjustment mode are provided in **4. Electrical Adjustments** in the Service Manual.)

8-2. Intermittent Operations of Servo

The focus servo and tracking servo of this unit turn ON and OFF repeatedly during normal playback and operate intermittently.
To save power, they repeat 1.8 seconds of ON and 2.8 seconds of OFF as shown in the timing chart in **Fig. 8-2.** along with the switching of the laser diode to ON/OFF. In the CLV servo, the control is different. When ON, as some time is required for the servo to stabilize, the disc is rotated continuously in the rough servo mode even when the focus servo and tracking servo are OFF. When the servo is ON, the focus servo sets the focus based on the focus voltage just before the servo is OFF to operate the focus servo circuit.

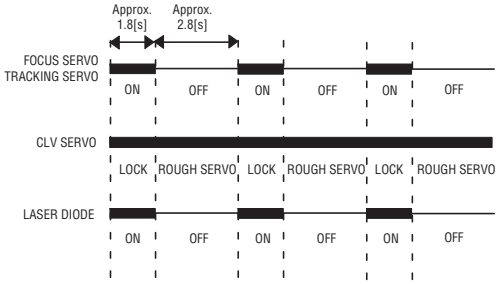


Fig. 8-2. Intermittent Operations of Servo

8-3. Focus Search and Disc Discrimination

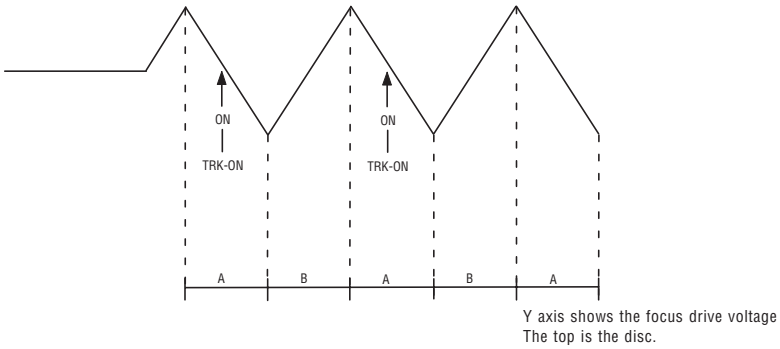


Fig. 8-3. Focus Search (Previous Model)

Compared to the current CD discs, as the reflection rate of the MO disc is low (15 to 30%), the difference between the pseudo reflected light on the disc surface (polycarbonate board surface of the side where signals are read) and the light reflected from the MO media side is small, making it difficult for the IC to differentiate between the two. As a result, the FOK signal sometimes becomes “H” according to the light reflected from the disc surface. Thus when the focus is turned ON, focus is accidentally imposed on the disc surface. Focus search is therefore performed from near the disc (down search) unlike current CDs to impose focus. (Part A of **Fig. 8-3.**)

In 4th generation playback only players, improvements of the optical block enabled detection of the MO media to be performed properly even when search was carried out from the far side of the disc as the disc surface deviated from the focusing range.
As shown in **Fig. 8-4.**, when search is performed from the side near the disc (down search), a disc with a high reflection rate (CD) is set, when search is performed from the side far away from the disc (up search), a disc with a low reflection rate (MO) is set, and MO/CD differentiation is performed together with focus search. After this, the focus on signal generated from the focus OK signal is used to turn ON the focus and tracking servos.

The following shows the focus search process and disc differentiation method of the 4th generation playback only player.

Focus search process and disc differentiation

(1) After the power is turned ON, first high reflection rate gain of the RF amplifier and laser power of the high reflection rate disc (CD) is set (0.6 mW), and focus search (from up to down) is started. (Part A of **Fig. 8-4.**)
(2) If this high reflection rate disc (CD) is loaded, focus is imposed. If a low reflection rate disc (MO) is loaded, focus is not imposed and the the idling state is set. (Part A of **Fig. 8-4.**)
(3) Search is performed once, and if the disc is not detected (if idling is set), the RF amplifier sets the low reflection rate gain again, sets the laser power of the low reflection rate disc (MO) (0.8 mW), and focus search (down to top) is performed. (Part B of **Fig. 8-4.**)
(4) If focus is imposed here, the disc is determined to be a low reflection rate disc (MO), after which the tracking servo turns ON and pit/groove differentiation is performed. This is performed by simultaneously switching the I+J (pit) and I-J (groove) of the RF signal output from the RF amplifier (IC501) and E-F (pit) and F-E (groove) of the tracking error signal using the pit/groove switching signal and detecting on which side the RF data is read.
(5) When the focus is not imposed (when the ABCD level does not reach a certain level), the above operation is retried till eight times.
(6) If focus is still not imposed after the retries, “NO DISC” is displayed.

* Disc differentiation is performed only once after the power is turned ON.

Immediately after the power turns ON, the offset data obtained in the adjustment mode and stored in the non-volatile memory (IC802, EEPROM) is sent to the servo circuit to perform correction. To correct the offset generated due to temperature characteristics, etc. of the optical block, fine adjustments of the focus offset and tracking offset are performed each time the unit is started.

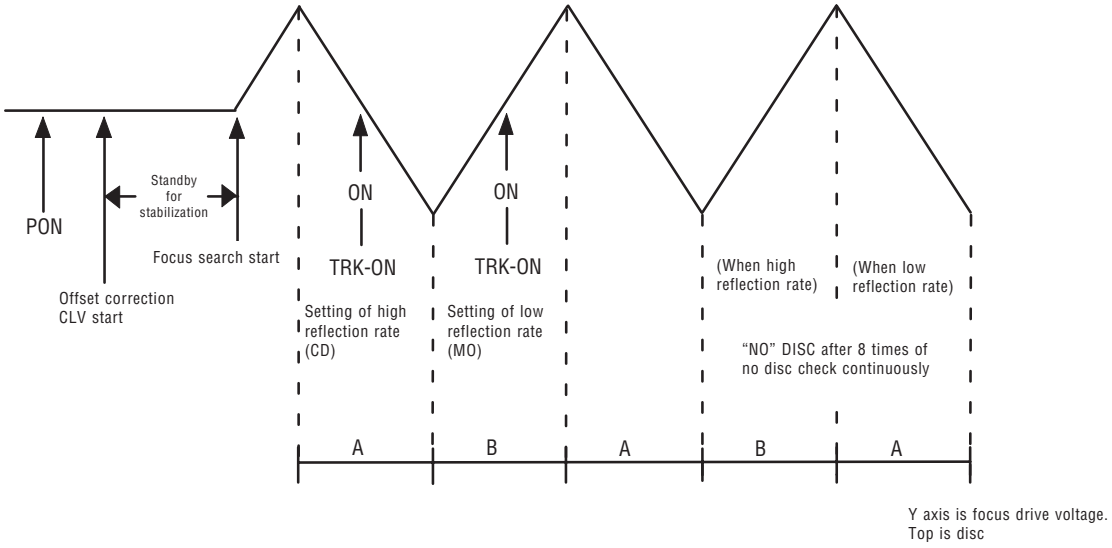


Fig. 8-4 Focus Search and Disc Differentiation (4th Generation Playback Only Player)

8-4. Focus Servo Circuit

As shown in **Fig. 8-5.**, the photoelectric current output from the optical block A to D detectors is input to the RF amplifier (IC501), converted to voltage by the I-V amplifier inside, passed through the ABCD amplifier and F.E. (focus error) amplifier, and the ABCD signal is output from Pin ㉟ (ABCD) while the focus error signal is output from Pin ㊱ (FE) to the DSP/digital servo (IC601). The A to D I-V amplifiers each have a gain switch for adjusting level. Using the serial data input from the system controller (IC801) via the serial bus (SBUS), initial settings of the gain is performed together with ABCD level adjustment according to the disc type each time PLAY, etc. to obtain the optimum output. To perform these, the system controller reads the ABCD level data A/D converted from the DSP/digital servo (IC601) and control the gain switch so that the data becomes the prescribed level.

The input of the DSP/digital servo (IC601) is incorporated with an A/D converter, which converts the ABCD signal and the FE signal to 7-bit data at sampling frequencies of 22.05 kHz (fs/2) and 88.2 kHz (2 fs) respectively. The focus error signal is then subject to servo calculation in the DSSP (digital servo signal processor) block, converted to the 88.2 kHz PWM wave, and used to control the focus coil via the servo driver (IC551) and LPF (low pass filter).
In addition to the ABCD level adjustment mentioned earlier, the A/D converted ABCD signal data is also compared with the reference level preset with the serial data from the system controller, and the FOK (focus OK) detection signal is output to the system controller via the serial bus (SBUS).
The focus gain and focus bias adjustments are performed in the adjustment mode, the adjustment values are stored in the non-volatile memory, the data is sent to the servo circuit via the serial bus (SBUS) at starting to set the focus gain and focus bias adjustment data. In the case of focus bias, data on the bias amount during adjustment is sent to the DSSP block, added to the focus error signal, and used to drive the focus coil.

8-5. Tracking Servo Circuit

As shown in the block diagram in **Fig. 8-6.**, the photoelectric current output from the E and F detectors of the optical block is input to Pins ① (IE) and ④ (IF) of the RF amplifier (IC501), and converted to voltage by the I-V amplifier.
The I-V amplifier is equipped with a switch for adjusting gain like the A to D I-V amplifiers of the focus servo circuit, and a F amplifier for adjusting E-F balance in the later stage of the I-V amplifier. These are set so that the optimum output is obtained according to the disc type (MO/CD) using the serial data input via the serial bus (SBUS) from the system controller (IC801), and the adjustment values obtained in the adjustment modes for EF gain and EF balance stored in the non-volatile memory (IC802, EEPROM) are used.

The T.E. (tracking error) amplifier inside the RF amplifier switches the internal circuit using the serial data from the system controller. The E-F tracking error signal is output in the case of pit while the F-E tracking error signal is output in the case of groove from Pin ㉝ (TE) based on the Vref voltage (0.88V) generated inside the RF amplifier. The tracking error signal input to the DSP/digital servo (IC601) is converted to 7-bit data at a sampling frequency of 88.2 kHz by the A/D converter inside. After servo calculation is performed by the DSSP block, the data is converted to 88.2 kHz PWM wave, and used to control the tracking coil via the servo driver (IC551) and LPF (low pass filter). In the adjustments of the tracking gain the adjustment data is stored in the non-volatile memory, and sent to the servo block inside the DSP/digital servo (IC601) via the serial bus (SBUS) from the system controller when the unit is started to optimize the servo. At the same time, automatic adjustment of the tracking offset is also performed each time the unit is started to correct the offset caused from the temperature characteristics of the optical block, etc.

8-6. Sled Servo Circuit

The bottom of **Fig. 8-6.** shows the block diagram of the sled servo circuit.
The tracking error data converted to 7-bit by the A/D converted inside the DSP/digital servo (IC601) is sent to the system controller (IC801) via the serial bus (SBUS). The system controller calculates the sledding distance using this data, etc., and outputs the control signal to the sled motor controller (IC803) composed of the gate array. The sled motor controller inputs this control signal and the back electromotive force generated in the motor coil while the sled motor is driven to the sled motor monitor (IC552) composed of the differential amplifier, additionally a monitor signal obtained in the circuit is input to the circuit. Inside the sled motor controller, timing is calculated using the control signal and monitor signal, the sled error signal is generated and used to drive the sled motor via the servo driver (IC551).

The power supply of the servo driver (IC551) used by the sled servo is controlled by the control signal output in the PWM wave from Pin ㊼ (SLD VCOM) of the system controller (IC801). When the sled motor is in the stop state, as Pin ㊼ is "L", Pin ㉚ (PO2) of the servo driver (IC551) also becomes "L", and power supplied to the H bridge driver in the servo driver is stopped. During driving, the voltage control signal in the PWM wave (2 fs=88.2 kHz) is output from Pin ㊼ of the system controller, the PWM driver of the servo driver performs switching, and power is supplied from Pins ㊵ and ㊷ to the H bridge driver via the LC filter.

When the power supply voltage drops, the duty ratio of the PWM wave output from Pin ㊼ of the system controller is made high to prevent the drop in the voltage added to the H bridge driver. If the power supply voltage drops considerably, the sled motor may not start in some cases due to the effects of the drop in the voltage of L556.
The output of Pin ㊽ (NC) of the system controller is set to "H", Q551 connected to the two ends of L556 are turned ON equivalently, and voltage of the battery is directly applied.

8-7. Spindle Servo Circuit

The spindle servo corresponds to the recording side of the disc as shown in **Table 8-1.**, and is divided broadly into the EFM-CLV and ADIP-CLV servo modes. In the pit area of the playback only disc (CD) and MO disc (PTOC), the EFM-CLV servo mode is used as in normal CD players. In the groove area of the MO disc, the ADIP-CLV servo mode is used.

Table 8-1. Spindle Servo Mode

Disc Type	Recording side	Servo Mode
MO groove	Groove	ADIP-CLV
MO pit (PTOC)	Pit	EFM-CLV
CD pit	Pit	EFM-CLV

As shown in the block diagram of the spindle servo in **Fig. 8-7.**, in the case of the EFM-CLV servo, the output of the I and J detectors is input to the RF amplifier (IC501). If the recording side is the pit area, the additional signal of I and J is output to the DSP/digital servo (IC601) from Pin ㊲ (RF-OUT) via the RF amplifier and EQ (equalizer) amplifier based on the Vref voltage (0.88V) generated inside the RF amplifier.
In the case of the ADIP-CLV servo, the wobbling components of the groove area obtained from the subtraction signal of the pushpull signals (A+D) and (B+C) of the main spot in the ADIP extraction circuit inside the RF amplifier (IC501) are output from Pin ㉙ (ADIP) as the binarized signal of the ADIP via the BPF (band pass filter).

The EFM or ADIP signal input to the DSP/digital servo (IC601) is converted to 7-bit data by the A/D converter, and used to perform reproduction of the clock in the PLL circuit. It is then passed through the switching circuit, and used for frequency division and for measuring the period in the counter. The data on the measured period data of the frequency division signal is then sent to the system controller via the serial bus (SBUS) from the DSP/digital servo.

The system controller also receives the U to W phase timing signals at Pins ㊷ to ㊹ (U MON to W MON) obtained from the back electromotive force generated in the motor coil during the rotation of the spindle motor by the 3-phase comparator inside the motor driver (IC551). Based on these inputs, the system controller performs servo calculation, generates the spindle error signal, outputs drive signals whose phase differ by 120° from Pins ㊺ to ㊼ (U CON to W CON), and drives the spindle motor via the 3-phase driver inside the servo driver (IC551).

During normal playback, as the laser diode, and focus and tracking servos turn ON and OFF intermittently, the EFM and ADIP signals are not obtained during the OFF period. During this time, the CLV servo estimates the target CLV speed of the track, at which the laser diode and servo turn ON and start reading, and drives the spindle motor using the rough servo.

The power supply of the servo driver (IC551) used by the spindle servo is controlled by the control signal output in the 88.2 kHz PWM wave from Pin ㊴ (CLV VCON) of the system controller.
When the spindle motor is started or the load is high, this PWM wave duty ratio is controlled so that it becomes high, and the voltage supplied to the 3-phase driver is made high to obtain a high rotation torque.

9. OPERATIONS OF MECHANISM

When disc door is opened

Open the disc door.

⬇

The switch lever pressed by the disc holder claw returns and moves in arrow direction Ⓐ.

⬇

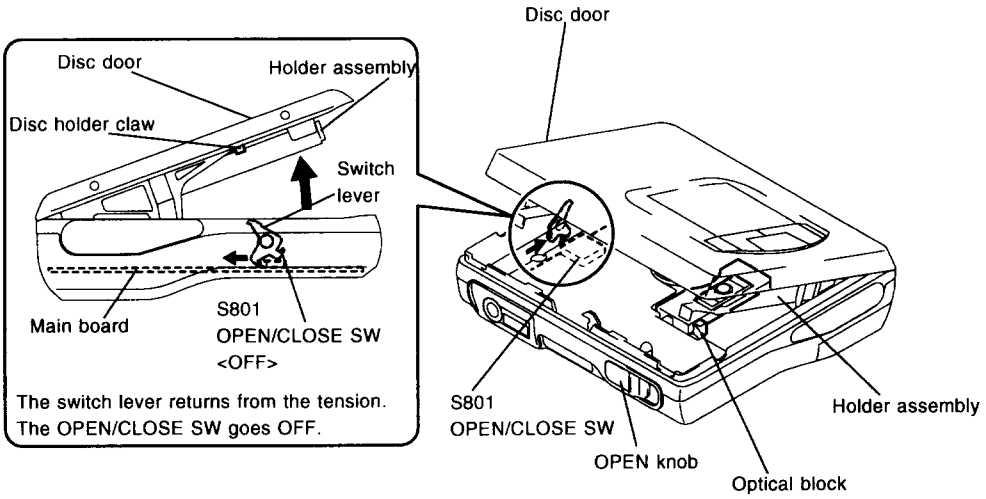
The OPEN/CLOSE SW (S801) goes OFF.

⬇

The optical block moves in the inner circumference.

⬇

The sleep mode is set and power supply is stopped.



When disc door is closed

Close the disc door.

⬇

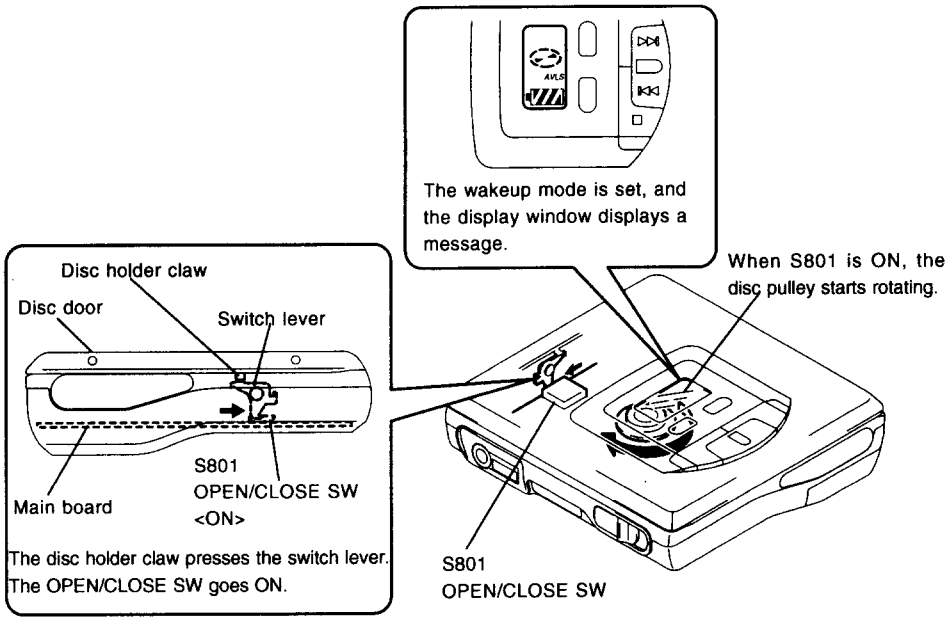
The switch lever is pressed by the disc holder claw, and moves in arrow direction Ⓑ.

⬇

The OPEN/CLOSE SW (S801) goes ON.

⬇

The wakeup mode is set, and the power supply circuit starts operating.

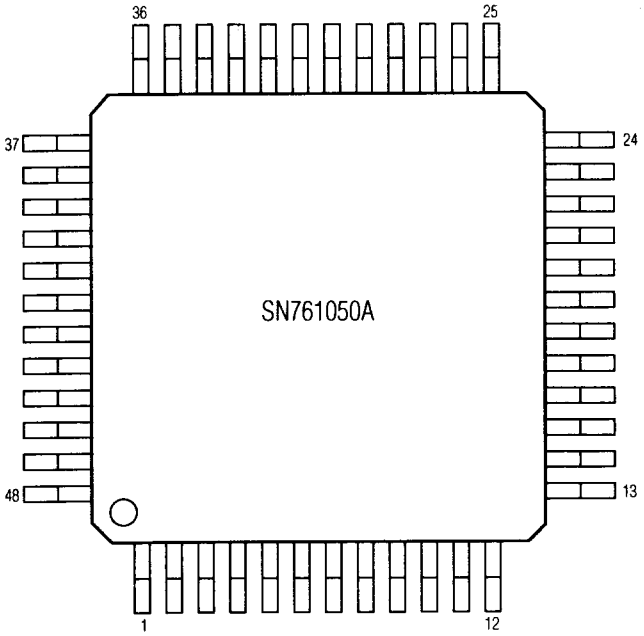

The wakeup mode is set, and the display window displays a message.
When S801 is ON, the disc pulley starts rotating.
Disc holder claw
Disc door
Switch lever
S801
OPEN/CLOSE SW
<ON>
Main board
The disc holder claw presses the switch lever.
The OPEN/CLOSE SW goes ON.
S801
OPEN/CLOSE SW

10. APPENDIX (SEMICONDUCTOR SPECIFICATIONS)

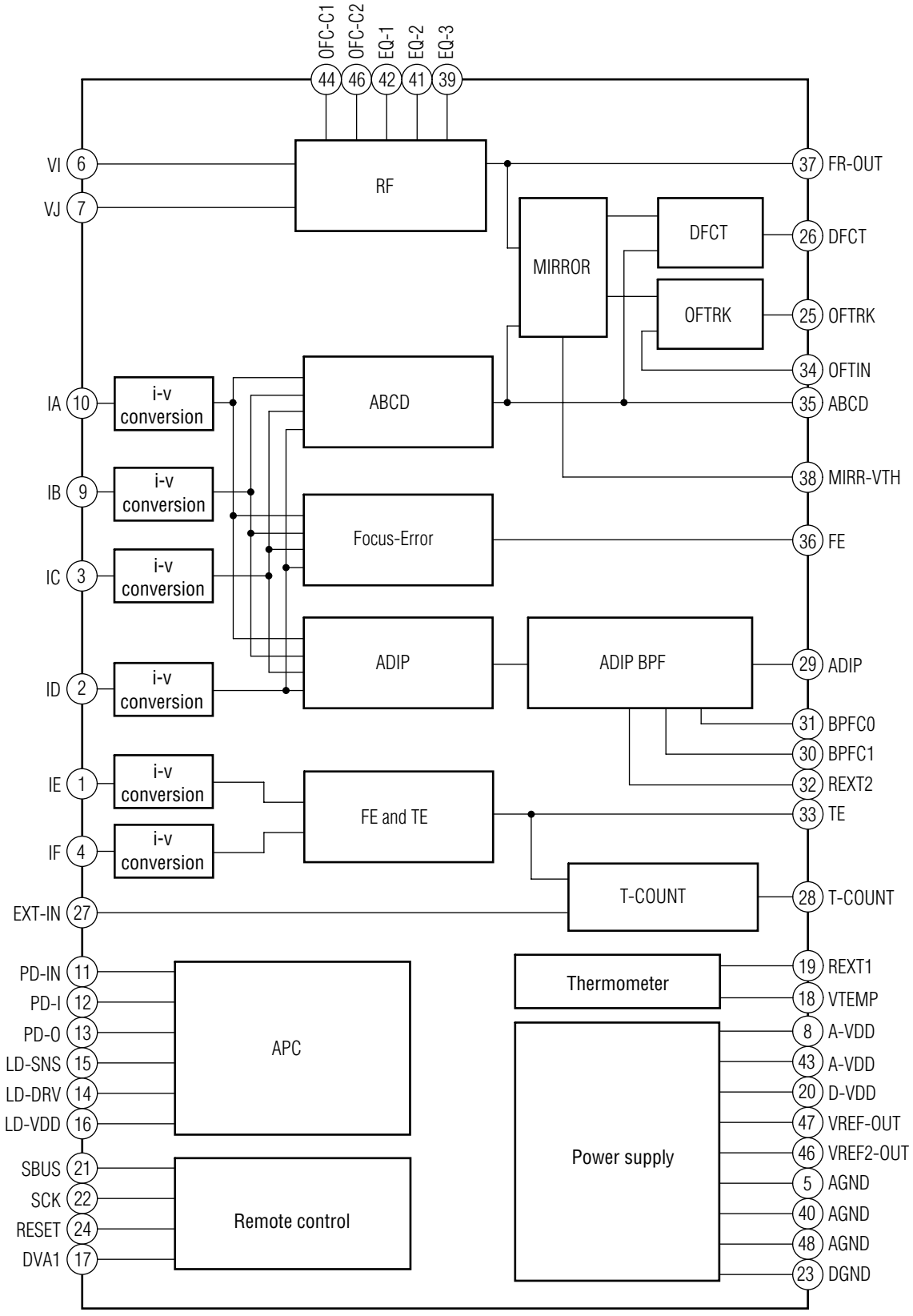
10-1. RF AMP SN761050A

RF amplifier for MD

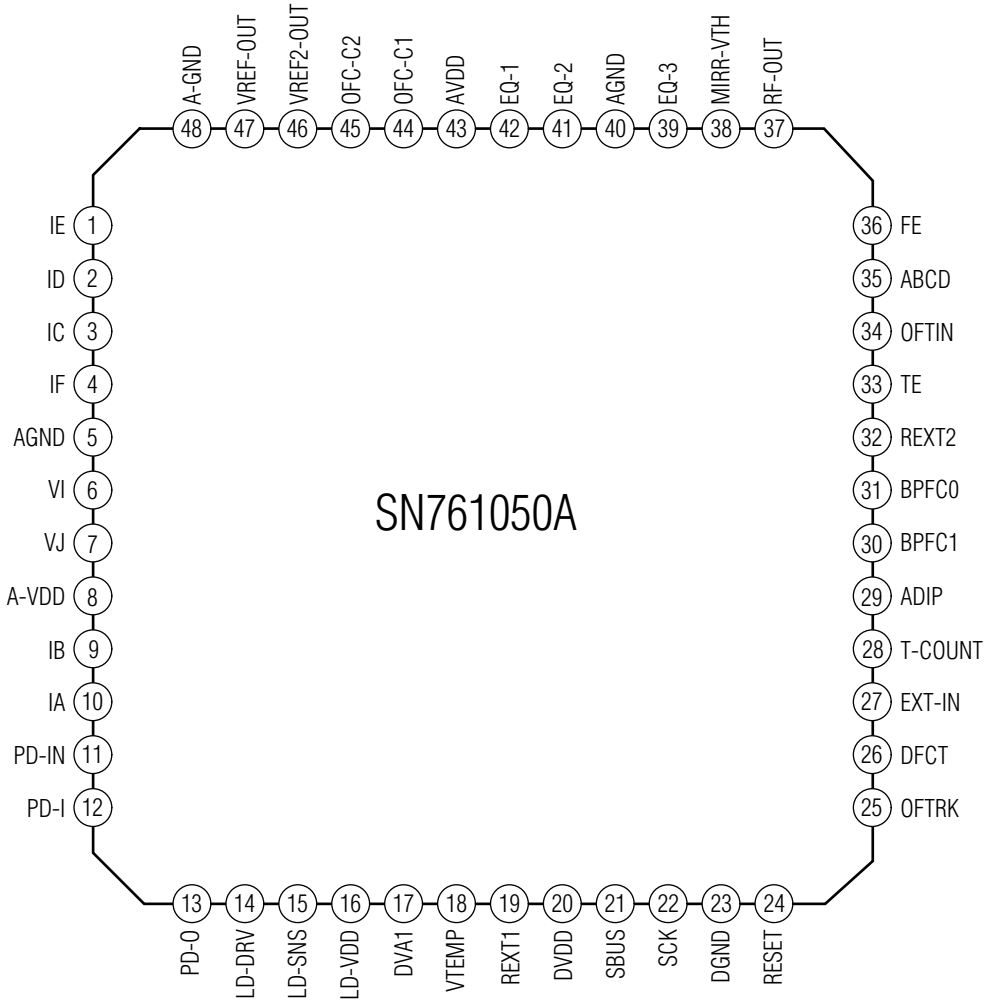
- Increasing adoption of parameter control method using serial interface.
- RF amplification, RF-EQ, tracking servo signal extraction, focus servo signal extraction, ADIP signal extraction functions
- MIRROR signal, OFTRK signal, DFCT signal, T-COUNT signal generation
- Incorporates APC circuit, thermometer function, reference voltage generation circuit



Internal Block Diagram



Pin Assignment



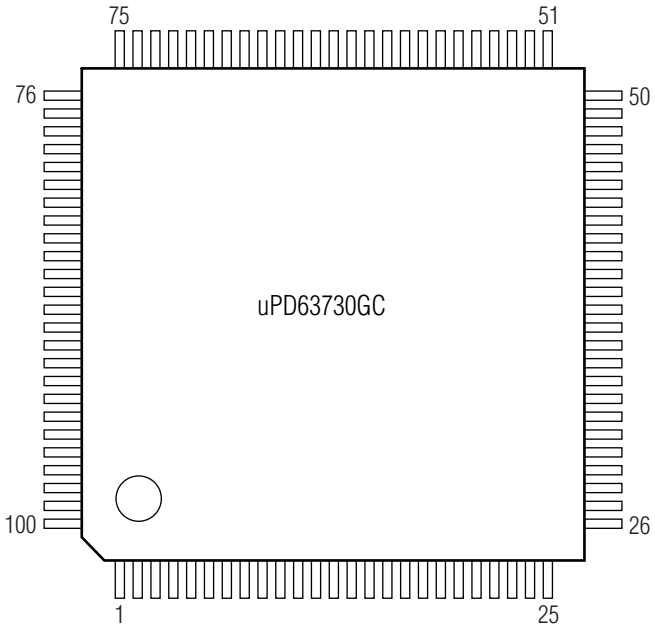
Pin Function

Pin No.	Symbol	I/O	Function
1	IE	I	E current input
2	ID	I	D current input
3	IC	I	C current input
4	IF	I	F current input
5	AGND	—	Analog GND
6	VI	I	I voltage input
7	VJ	I	J voltage input
8	A-VDD	—	Analog Vdd
9	IB	I	B current input
10	IA	I	A current input
11	PD-IN	I	PD AMP non-inverted input
12	PD-I	I	PD AMP inverted input
13	PD-O	O	PD AMP output
14	LD-DRV	O	LD-driver PNP-Tr base output
15	LD-SNS	I	LD current detection input
16	LD-VDD	I	LD power supply voltage detection input
17	DVA1	I	Serial device code
18	VTEMP	O	Temperature gauge output
19	REXT1	—	Temperature gauge current source setting resistor
20	DVDD	—	Digital Vdd
21	SBUS	I	Serial data input
22	SCK	I	Serial clock input
23	DGND	—	Digital GND
24	RESET	I	Reset input
25	OFTRK	O	Off track detection output
26	DFCT	O	Defect detection output
27	EXT-IN	I	External T-COUNT input
28	T-COUNT	O	T-COUNT output
29	ADIP	O	ADIP output
30	BPFC1	—	ADIP-BPF AC connecting capacitor
31	BPFC0	—	ADIP-BPF AC connecting capacitor
32	REXT2	—	ADIP-BPF current source setting resistor
33	TE	O	Tracking error output
34	OFT-IN	I	Off track detection input
35	ABCD	O	A+B+C+D output
36	FE	O	Focus error output
37	RF-OUT	O	RF output
38	MIRR-VTH	I	Mirror comparator threshold setting
39	EQ-3	—	RF-amp phase shifter
40	AGND	—	Analog GND
41	EQ-2	—	RF-EQ external constant 2
42	EQ-1	—	RF-EQ external constant 1
43	AVDD	—	Analog Vdd
44	OFC-C1	—	DC canceler external capacitor 1
45	OFC-C2	—	DC canceler external capacitor 1
46	VREF2-OUT	O	Reference voltage output (GND reference 1.2V)
47	VREF-OUT	O	Reference voltage output (GND reference 1.2V)
48	AGND	—	Analog GND

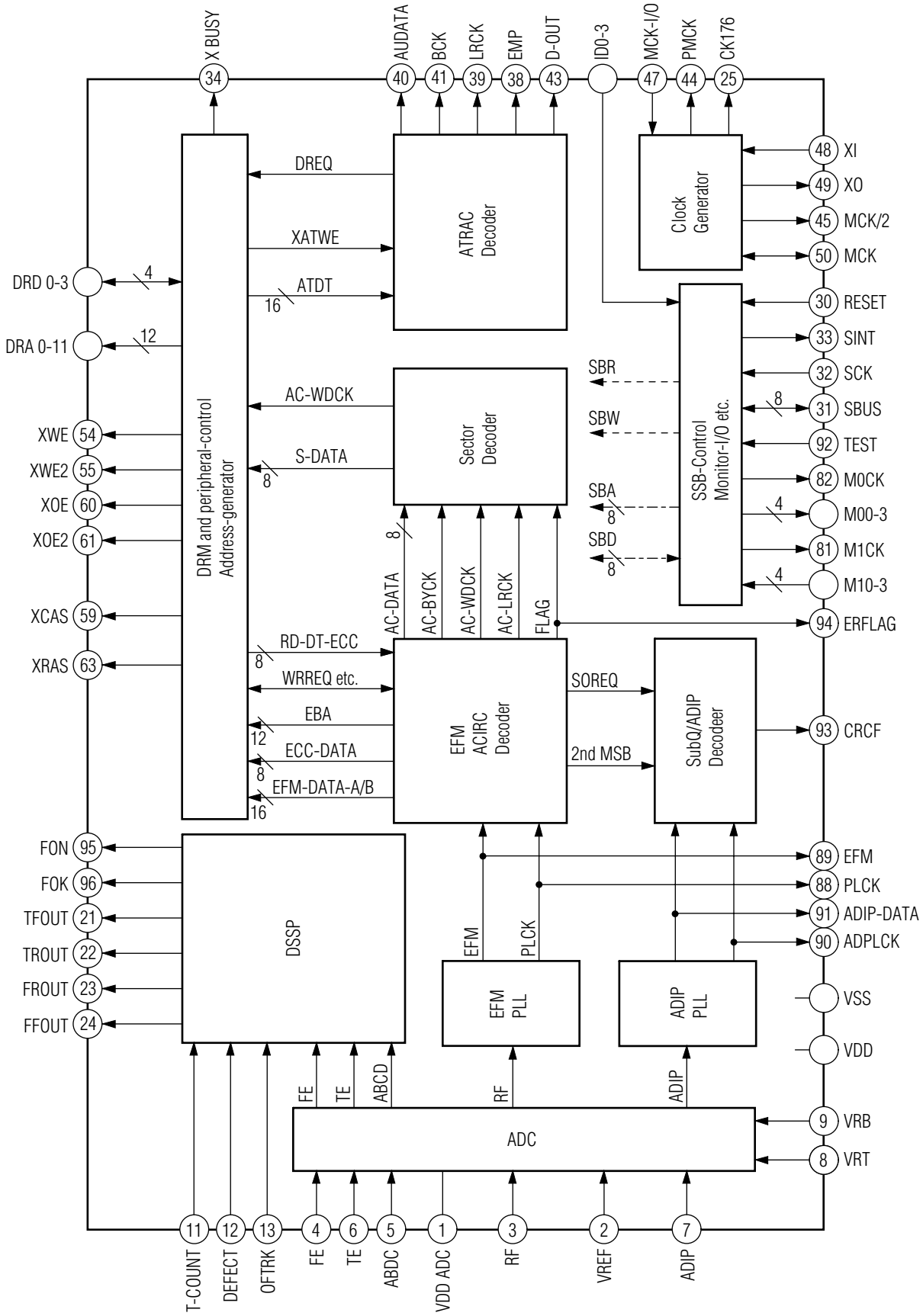
10-2. DSP/Digital Servo µPD63730GC

DSP/digital servo for MD playback

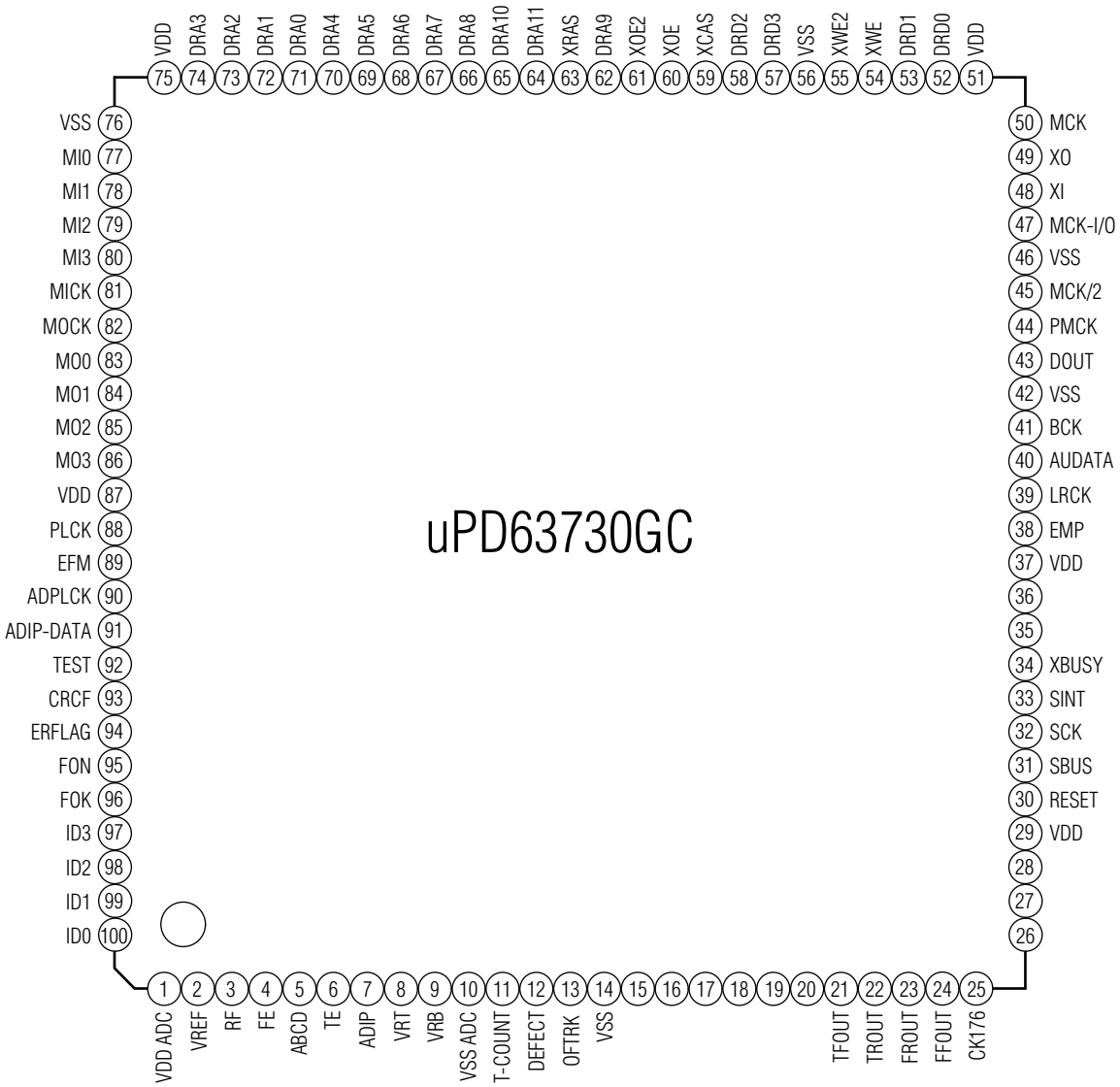
- Built-in ATRAC decoder for playback
- Digital servo, EFM decoder, and ACIRC decoder functions



Internal Block Diagram



Pin Configuration



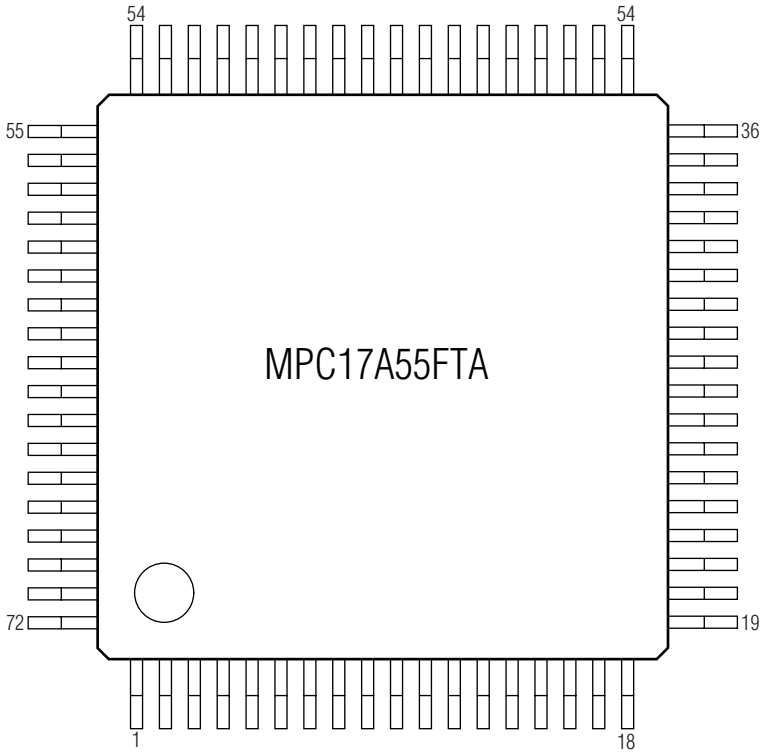
Pin Function

Pin No.	Symbol	I/O	Function
1	VDD ADC	—	Power supply for ADC block
2	VREF	I	Reference voltage input
3	RF	I	RF signal input
4	FE	I	Focus error input
5	ABCD	I	ABCD (all quantity of light) signal input
6	TE	I	Tracking error input
7	ADIP	I	ADIP signal input
8	VRT	I	ADC high potential reference voltage for RF
9	VRB	I	ADC low potential reference voltage for other than RF
10	VSS ADC	—	Ground for ADC block
11	T-COUNT	I	Tracking count signal input
12	DEFECT	I	Defect signal input
13	OFTRK	I	Off track signal input
14	VSS	—	Ground
15			
16			
17			
18			
19			
20			
21	TFOUT	O	Tracking servo output (1)
22	TROUT	O	Tracking servo output (2)
23	FROUT	O	Focus servo output (1)
24	FFOUT	O	Focus servo output (2)
25	CK176	O	176.4 kHz (4 fs) output
26			
27			
28			
29	VDD	—	Power supply
30	RESET	I	Reset input. Reset when “L”.
31	SBUS	I/O	SBUS interface input/output
32	SCK	I	SBUS clock input
33	SINT	O	Interrupt signal output
34	XBUSY	O	DRAM access status
35			
36			
37	VDD	—	Power supply
38	EMP	O	Emphasis output for DAC. ON when ‘H”.
39	LRCK	O	L/R clock output
40	AUDATA	O	Audio data output
41	BCK	O	Bit clock output
42	VSS	—	Ground
43	DOUT	O	Digital output
44	PMCK	O	1/4 divided output of MCK
45	MCK/2	O	1/2 divided output of MCK
46	VSS	—	Ground
47	MCK I/O	I	Input/output direction switching of MCK. “L”:output, “H”:input.
48	XI	I	Crystal oscillation input (384 fs=16.93 MHz)
49	XO	O	Crystal oscillation output
50	MCK	I/O	Master clock input/output

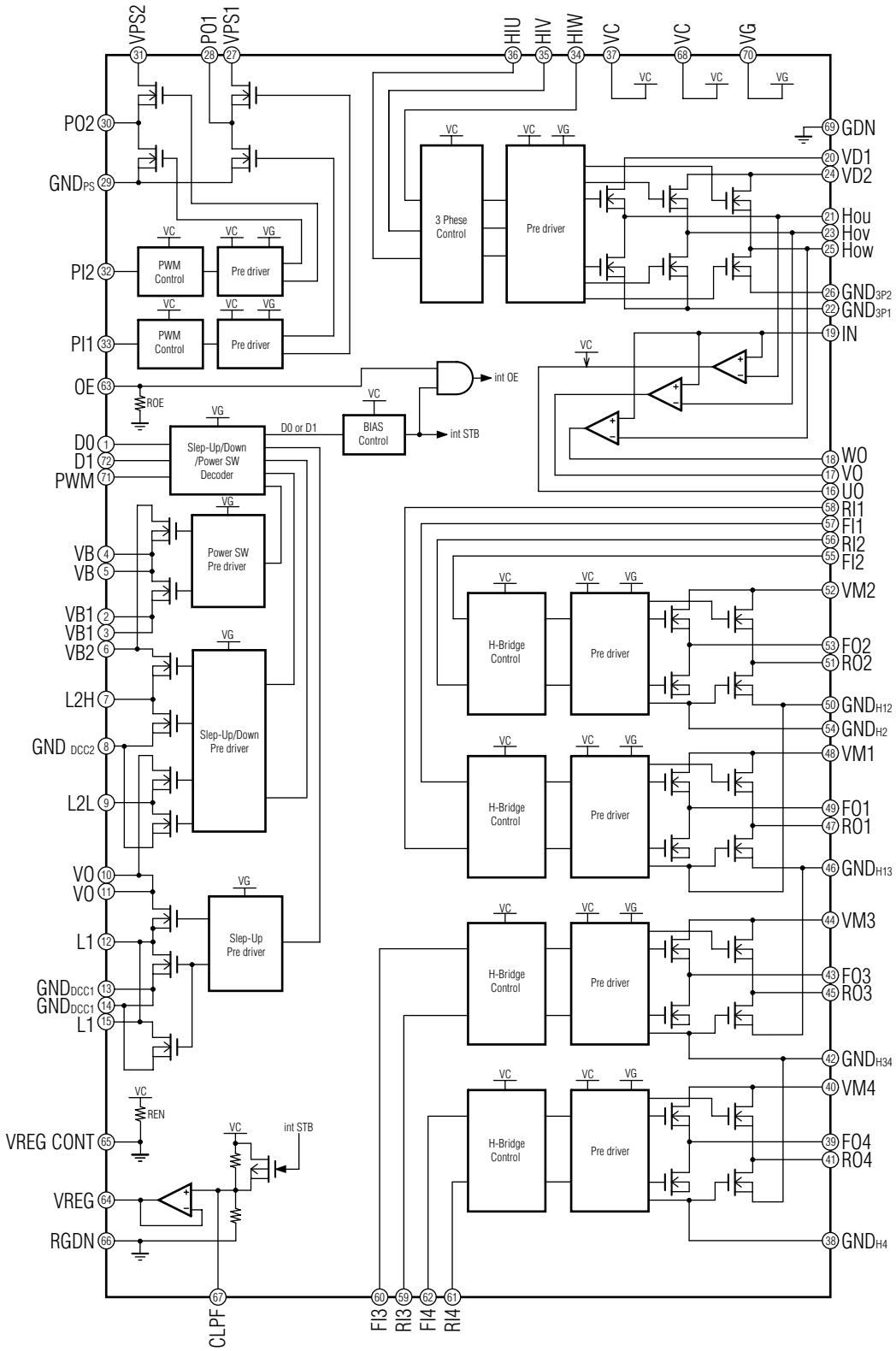
Pin No.	Symbol	I/O	Function
51	VDD	—	Power supply
52	DRD0	I/O	DRAM data input/output
53	DRD1	I/O	DRAM data input/output
54	XWE	O	DRAM write enable output
55	XWE2	O	DRAM write enable output
56	VSS	—	Ground
57	DRD3	I/O	DRAM data input/output
58	DRD2	I/O	DRAM data input/output
59	XCAS	O	DRAM-CAS output
60	XOE	O	DRAM output enable output
61	XOE2	O	DRAM output enable output
62	DRA9	O	DRAM address output
63	XRAS	O	DRAM-RAS output
64	DRA11	O	DRAM address output
65	DRA10	O	DRAM address output
66	DRA8	O	DRAM address output
67	DRA7	O	DRAM address output
68	DRA6	O	DRAM address output
69	DRA5	O	DRAM address output
70	DRA4	O	DRAM address output
71	DRA0	O	DRAM address output
72	DRA1	O	DRAM address output
73	DRA2	O	DRAM address output
74	DRA3	O	DRAM address output
75	VDD	—	Power supply
76	VSS	—	Ground
77	M10	I/O	Monitor input
78	M11	I/O	Monitor input
79	M12	I/O	Monitor input
80	M13	I/O	Monitor input
81	MICK	O	Monitor in clock
82	MOCK	O	Monitor out clock
83	M00	O	Monitor output
84	M01	O	Monitor output
85	M02	O	Monitor output
86	M03	O	Monitor output
87	VDD	—	Power supply
88	PLCK	I/O	PLL clock input/output
89	EFM	I/O	PLL input/output
90	ADPLCK	I/O	ADIP-PLL clock input/output
91	ADIP-DATA	I/O	ADIP-PLL demodulation input/output
92	TEST	I	Test
93	CRCF	O	CRC flag
94	ERFLAG	O	Error flag
95	FON	O	FON signal
96	FOK	O	FOK signal
97	ID3	I	SSB code setting input
98	ID2	I	SSB code setting input
99	ID1	I	SSB code setting input
100	ID0	I	SSB code setting input

10-3. Servo Driver MPC17A55FTA

MD/CD player motor driver, system power supply



Internal Block Diagram



Pin Function

Pin No.	Symbol	I/O	Function
1	D0	I	Operation mode setting
2	VB1	I	Power switch input 1
3	VB1	I	Power switch input 1
4	VB	O	Power switch output
5	VB	O	Power switch output
6	VB2	I	Power switch input 2
7	L2H	O	Step up/down converter PWM output
8	GND DCC2	—	Step up/down converter GND
9	L2L	O	Step up/down converter fixed pulse output
10	VO	O	DC/DC converter output
11	VO	O	DC/DC converter output
12	LI	O	Step up converter PWM output
13	GND DCC1	—	Step up converter power GND
14	GND DCC1	—	Step up converter power GND
15	L1	O	Step up converter PWM output
16	UO	O	U phase output of the phase detection comparator
17	VO	O	V phase output of the phase detection comparator
18	WO	O	W phase output of the phase detection comparator
19	IN	I	Normal rotation input of the phase detection comparator
20	VD1	—	Three-phase driver power supply
21	HOU	O (I)	Three-phase driver U phase output and reverse rotation input of the phase detection comparator
22	GND3P1	—	Power GND for the three-phase driver
23	HOV	O (I)	Three-phase driver V phase output and reverse rotation input of the phase detection comparator
24	VD2	—	Power supply of the three-phase driver
25	HOW	O (I)	Three-phase driver W phase output and reverse rotation input of the phase detection comparator
26	GND 3P2	—	Power GND for the three-phase driver
27	VPS1	—	PWM driver 1 power supply
28	PO1	O	PWM driver 1 output
29	GND PS	—	Power GND for PWM driver
30	PO2	O	PWM driver 2 output
31	VPS2	—	PWM driver 2 power supply
32	PI2	I	PWM driver 2 control input
33	PI1	I	PWM driver 1 control input
34	HIW	I	Three-phase driver control input
35	HIV	I	Three-phase driver control input
36	HIU	I	Three-phase driver control input
37	VC	—	Control circuit power supply
38	GND H4	—	Power GND for the H bridge driver
39	FO4	O	H bridge driver 4 output
40	VM4	—	H bridge driver 4 power supply
41	RO4	O	H bridge driver 4 output
42	GND H34	—	Power GND for the H bridge driver
43	FO3	O	H bridge driver 3 output
44	VM3	—	H bridge driver 3 power supply
45	RO3	O	H bridge driver 3 output

Pin No.	Symbol	I/O	Function
46	GND H13	_	Power GND for the H bridge driver
47	RO1	O	H bridge driver 1 output
48	VM1	_	H bridge driver 1 power supply
49	FO1	O	H bridge driver 1 output
50	GND H12	_	Power GND for the H bridge driver
51	RO2	O	H bridge driver 2 output
52	VM2	_	H bridge driver 2 power supply
53	FO2	O	H bridge driver 2 output
54	GND H2	_	Power GND for the H bridge driver
55	FI2	I	H bridge driver 2 control input
56	RI2	I	H bridge driver 2 control input
57	RI1	I	H bridge driver 1 control input
58	RI1	I	H bridge driver 1 control input
59	RI3	I	H bridge driver 3 control input
60	FI3	I	H bridge driver 3 control input
61	RI4	I	H bridge driver 4 control input
62	FI4	I	H bridge driver 4 control input
63	OE	I	Driver output enable control input
64	VREG	O	Regulator circuit output
65	VREG CONT	I	Regulator circuit output enable control input
66	RGND	_	Regulator circuit GND
67	CLPF		Regulator circuit reference voltage filter
68	VC	_	Control circuit power supply
69	GND	_	Control circuit GND
70	VG	_	Pre-driver circuit power supply
71	PWM	I	DC/DC PWM signal input
72	D1	I	Operation mode setting

Outline of Operations

(1) Power Switch, DC/DC Block

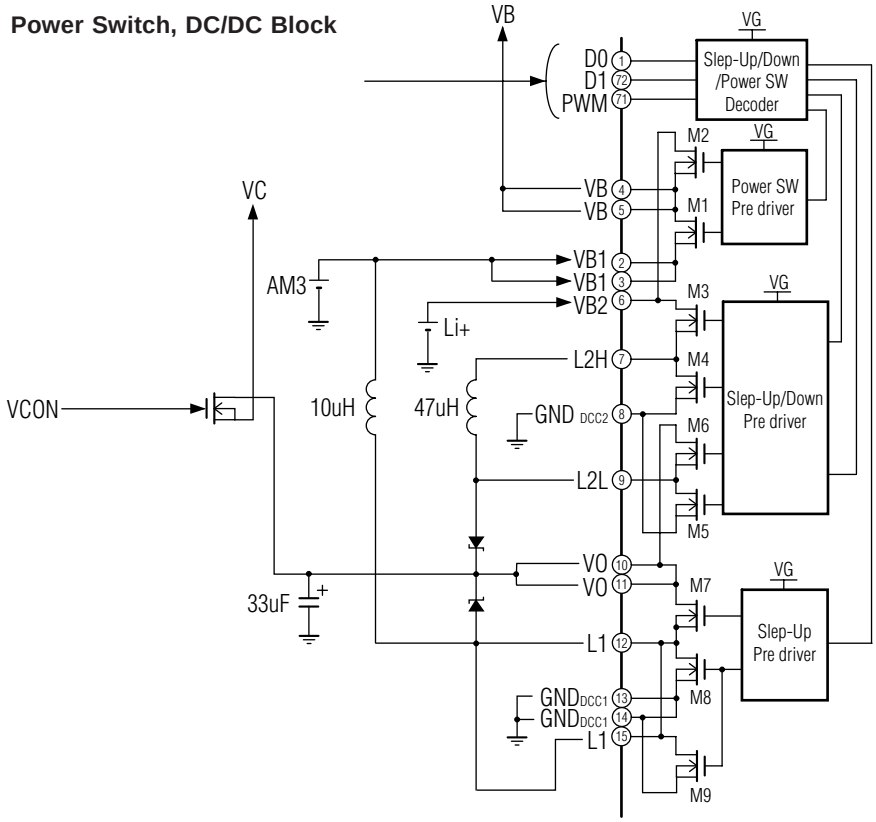


Fig. 1 Power Switch, DC/DC Section

As shown in Truth Table 1, in the power switch, the VB1 and VB2 voltages are output to the VB terminal by the combination of D0 and D1. The power MOS making up the switch has an approximately 0.2 Ω ON resistor which can output current up to 600 mA. However, as this power MOS also incorporates a parasitic PN junction diode from the source to the drain, the VB2 voltage must be higher than VB1–0.5V.

The DC/DC section can be combined with MPC1830 to construct a switching regulator. MPC1830 determines the operation mode while monitoring VB1, VB2, and the output voltage VC, and outputs the voltage as D0 and D1. By the combination of D0 and D1, the operations of the power-MOSFET are set as shown in Truth Table 2. “PWM” and “PWMB” in the table indicate outputs with the same phase and opposite phase with the 176 kHz PWM signal input to the PWM terminal are obtained respectively. a 176 kHz, duty 70% fixed pulse is also output
to the L2L terminal.

Truth Table 1 (Power Switch)

D0	D1	M1	M2	VB
L	L	OFF	OFF	Z
L	H	ON	OFF	VB1
H	L	OFF	ON	VB2
H	H	OFF	ON	VB3

Truth Table 2 (Power Switch)

D0	D1	M7	M8, 9	L1	M3	M4	L2H	M6	M5	L2L	
L	L	OFF	OFF	Z	OFF	OFF	Z	OFF	OFF	Z	* Standby state
L	H	PWMB	PWM	PWMB	OFF	OFF	Z	OFF	OFF	Z	* Step-up
H	L	OFF	OFF	Z	PWM	PWM	PWM	ON	OFF	VO	* Step-down
H	H	OFF	OFF	Z	PWM	PWM	PWM	70%	30%	70%	* Step-up/down

(2) Bias control block

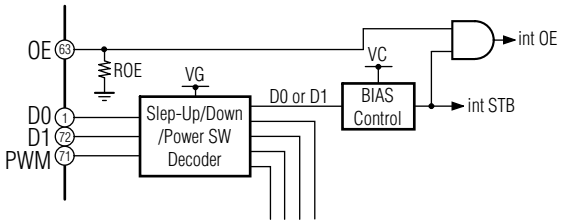


Fig. 2 Bias operation Block

The two signals Int STB, Int OE shown in the truth table are made from the D0, D1, OE, and VC voltages. These two signals are not output to outside, and are used to switch the power switch, circuit blocks other than the DC/DC block to the standby or operating state. The bias control circuit when D0 or D1 is “H” contains hysteresis, so that at the rising edge of VC, Int STB changes from “L” to “H” at 2.1V, and at the falling edge of VC, it changes from “H” to “L” at 1.4V.

Truth Table

D0 or D1	OE	VC	Int STB	Int OE
L	X	X	L	L
H	X	Below 1.4V	L	L
H	L	Above 2.1V	H	L
H	H	Above 2.1V	H	H

(3) H bridge driver

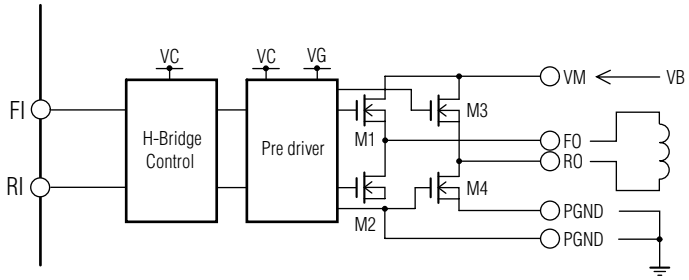


Fig. 3 H Bridge Driver

H bridge drivers with different ON resistors and logic are incorporated in four channels. These set into the standby state when Int OE is “L”, and their outputs are fixed at “L” regardless of the input logic. When Int OE becomes “H”, these drivers starts operating. The ON resistor is defined as the sum of the top and bottom.

Channel	Symbol	Value (typ.)
1, 3	RON1, 3	0.6Ω
2, 4	RON2, 4	1.0Ω

Truth Table

Int OE	FI	RI	FO1, 3	RO1, 3	FO2, 4	RO2, 4
L	X	X	L	L	L	L
H	L	L	L	L	L	L
H	L	H	L	H	L	H
H	H	L	H	L	H	L
H	H	H	L	L	Z	Z

(4) 3-Phase Driver

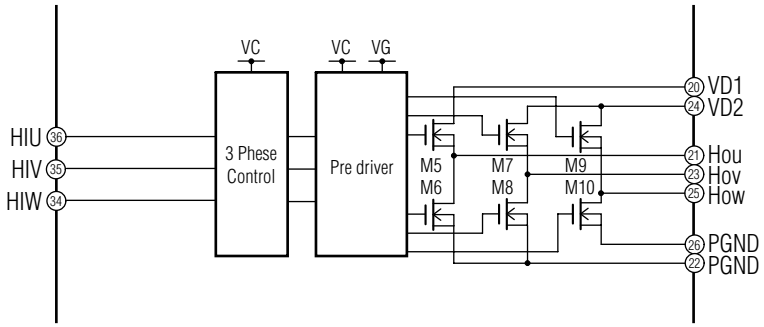


Fig. 4 3-Phase Driver

The 3-phase motor driver is composed of three half-bridges. This driver also sets into the standby state when Int OE is “L”, and its output is fixed at “L” regardless of the input logic. When Int OE becomes “H”, the driver sets into the operating state. The ON resistors M5 to M10 are each 0.5 Ω (typ.).

Truth Table

Int OE	HIU	HIV	HIW	HOU	HOV	HOW
L	X	X	X	L	L	L
H	L	L	L	L	L	L
H	L	L	H	Z	L	H
H	L	H	L	L	H	Z
H	L	H	H	L	Z	H
H	H	L	L	H	Z	L
H	H	L	H	H	L	Z
H	H	H	L	Z	H	L
H	H	H	H	L	L	L

(5) PWM Drivers 1, 2

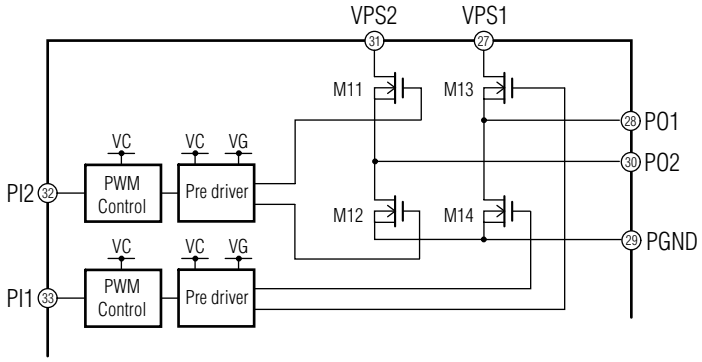


Fig. 5 PWM Driver

The PWM driver is a half-bridge driver with 2 channels with different ON resistors. It sets into the standby state when Int OE is “L”, and sets into the operating state when the signal becomes “H”. The ON resistors M11 and M12 are 1.0 Ω (typ.) and M13 and M14 are 0.5 Ω (typ.).

Truth Table

Int OE	PI1, 2	PO1, 2
L	X	L
H	L	L
H	H	H

(6) 3-Phase Comparator

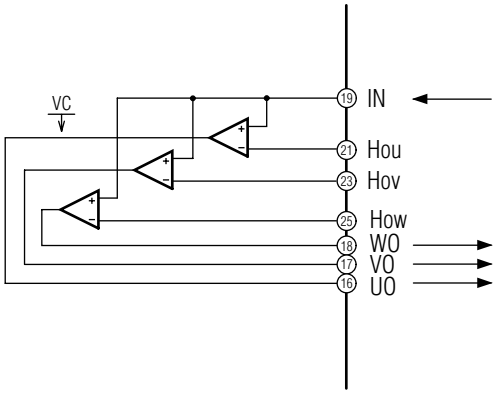


Fig. 6 3-Phase Comparator

This comparator is used for detecting the phase of the 3-phase motor driver. The IN terminal of one pin is commonly used for + input terminal. – input terminal is commonly used for each of the three 3-phase driver outputs. When the Int STB signal is "L", the output is fixed at "L", and operates at "H". The 3-phase comparator does not affect the OE terminal.

Functions Table

Int STB	U, V, WO
L	L
H	Comparator operations

(7) Regulator (VREG)

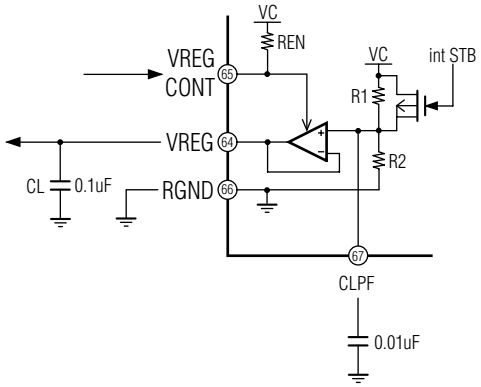


Fig. 7 Regulator (VREG)

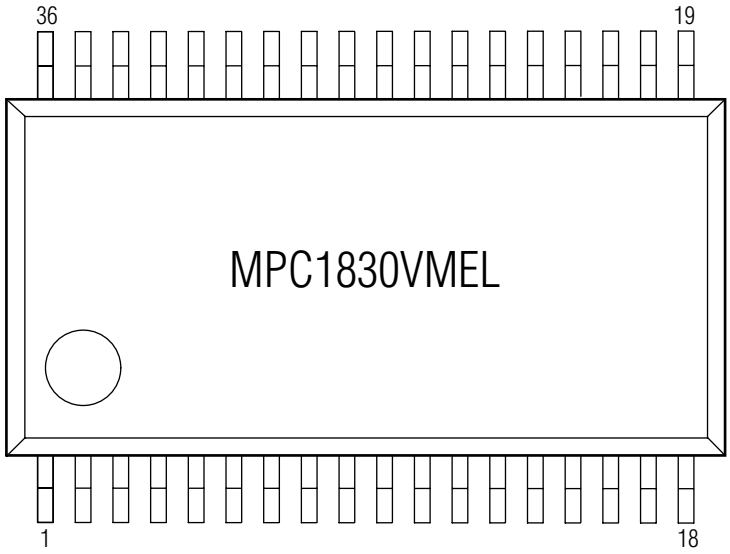
A voltage follower with a input voltage in which VC is divided by R1 and R2 is provided. The ratio of R1 (28 kΩ) to R2 (252 kΩ) is 1:9, and a 0.9 ×VC voltage is input to the voltage follower. As the CFPF terminal is equipped with a capacitor to form a LPF, affects by VC ripples, etc. are reduced. At the rising edge of VC, the PMOS mounted in a parallel with R1 remains ON while Int STB is "L" to speed up the rising time of the CLPF terminal. The voltage follower sets into the standby state when the OR of D0 and D1 is "L". Its output then becomes High-Z, and it starts operating at "H". While the voltage follower is operating, the mode is switched according to the VC voltage level and VREG CONT terminal. As described in the bias control section, as Int STB contains hysteresis against VC, when VC rises, VREG switches from VC to 0.9 ×VC at 2.1V. When it falls, VREG switches from 0.9 ×VC to VC at 1.4V. When VREG CONT is "L", VREG becomes High-Z.

Functions Table

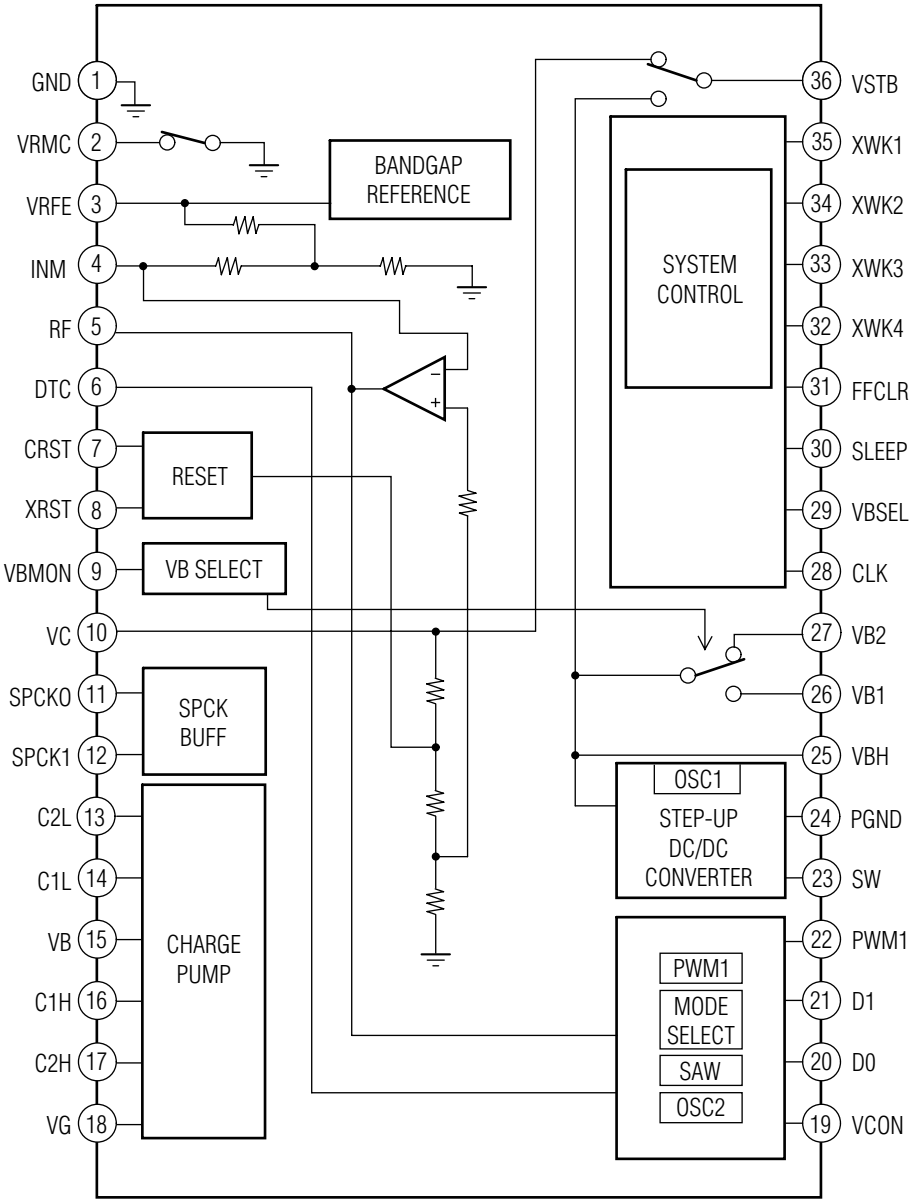
D0 or D1	VC	VREG CONT	VREG
L	X	X	Z
H	Below 1.4V	L	Z
H	Below 1.4V	H	VC
H	Above 2.1V	L	Z
H	Above 2.1V	H	0.9VC

10-4. DC-DC Converter MPC1830VMEL

Power Supply for System for MD/CD Player



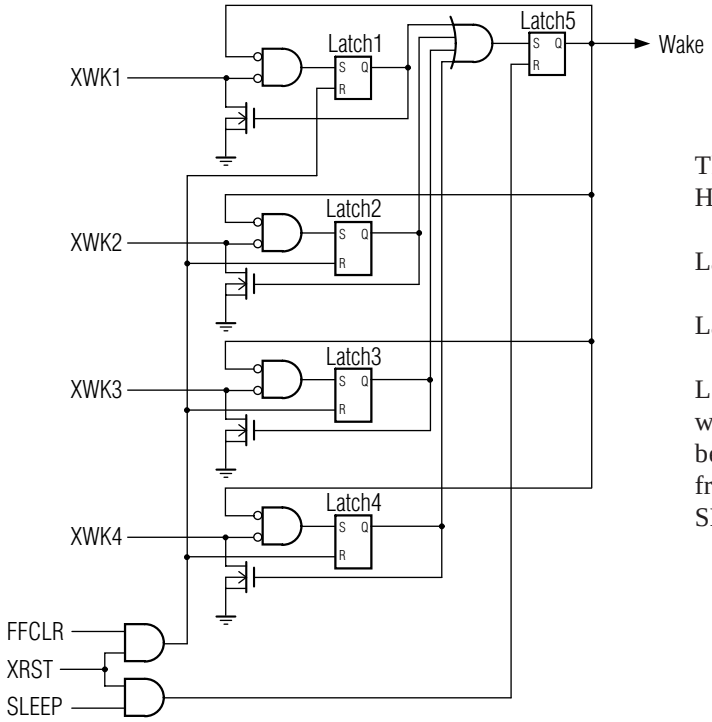
Internal Block



Pin Functions

Pin No.	Symbol	I/O	Function
1	GND	I	GND pin of control block
2	VRMC	O	SW output for remote commander
3	VREF	O	Connected to capacitor for reference voltage output pin filter.
4	INM	I	Switching power supply control circuit error amplifier inverted input pin
5	RF	O	Switching power supply control circuit error amplifier feedback resistor connection output pin
6	DTC	I	Switching power supply control circuit dead time control pin
7	CRST	I	Reset circuit reset signal delay capacitor connection pin
8	XRST	O	Reset circuit reset signal output pin. Monitors the VC voltage
9	VBMON	O	VB1, VB2 switching monitor output pin
10	VC	I	VC control voltage input pin
11	SPCKO	O	Clock driver output for external power supply
12	SPCKI	I	Clock driver input for external power supply
13	C2L	O	Capacitor connection pin for charge pump:(–) pole
14	C1L	O	Capacitor connection pin for charge pump:(–) pole
15	VB	I	Power input pin for charge pump
16	C1H	O	Capacitor connection pin for charge pump:(+) pole
17	C2H	O	Capacitor connection pin for charge pump:(+) pole
18	VG	O	Voltage output pin for charge pump. Connected to smoothing capacitor.
19	VCON	O	Switching power supply control driver start request output
20	D0	O	Switching power supply control mode output
21	D1	O	Switching power supply control mode output
22	PWM1	O	Switching power supply control PWM output
23	SW	O	Stepup converter driver pin
24	PGND	I	Driver output grounding pin
25	VBH	O	Outputs the higher voltage between the VB1 and VB2 inputs. Connected to smoothing capacitor
26	VB1	I	Pin connecting 1 cell (1.5V) batteries such as Ni-cd, Ni-MH batteries
27	VB2	I	Lithium ion battery connection pin
28	CLK	I	External clock input pin for sync control
29	VBSEL	I	Primary side power supply switching input pin
30	SLEEP	I	Sleep signal input pin
31	FFCLR	I	Input latch clear input pin for start signal
32	XWK4	I	Start signal input pin
33	XWK3	I	Start signal input pin
34	XWK2	I	Start signal input pin
35	XWK1	I	Start signal input pin
36	VSTB	O	Operating power supply output pin. Outputs power supply voltage during operations

Outline of Operations



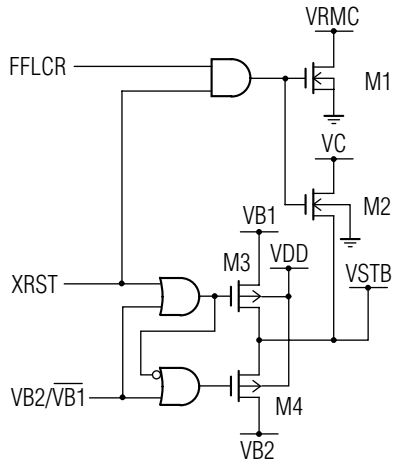
Start operation Input Circuit

The start circuit operates when the wake terminal becomes HIGH.

Latches at the rising edge of Latch 1 to 4.

Latches when Latch 5 becomes H from L.

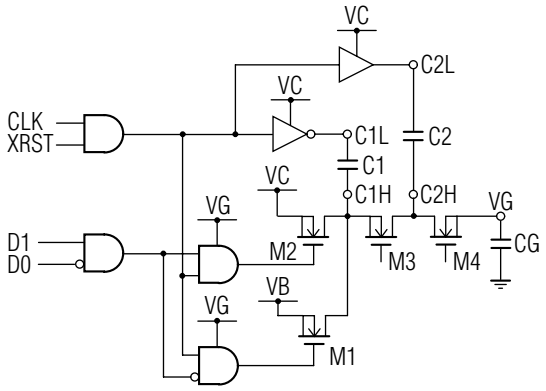
Latching is set at the falling edge of XWK1 to XWK4, and wake is output. At this time, the input terminal which had become LOW prohibits the latching of other input terminals from being set until FFCLR becomes HIGH. The FFCLR and SLEEP terminals are negated while XRST is LOW.



Standby Power Supply Generation Circuit

VDD is always output with the highest voltage from amongst VB1, VB2, and VC.

When XRST is LOW, M1 and M2 go OFF, and when VB2/VB1 is LOW, M3 becomes OFF, and M4 becomes ON. When XRST becomes HIGH, M3 and M4 go OFF, and M1 and M2 turn ON.

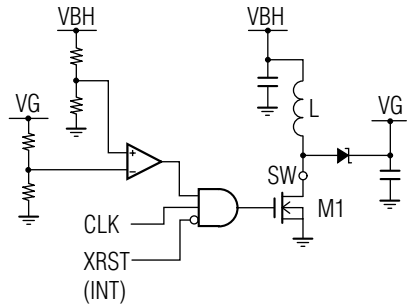


Charge Pump Circuit

When XRST is H, D0 becomes L and D1 becomes H, and M2 turns ON, and M1 goes OFF.
When D0 becomes H, M2 goes OFF, and M1 turns ON.

When D0:L D1:H (using VB1)
VG=3×VC

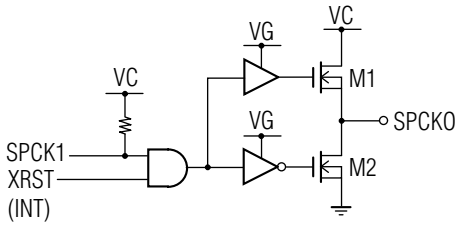
When D0:H D1:H or L (using VB2)
VG=VB+2×VC



VG Generation Circuit for Starting

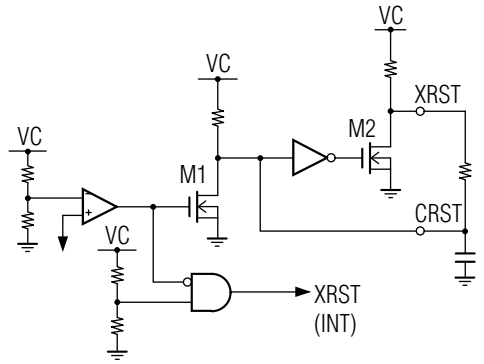
VBH is output with the higher voltage between VB2 and VB1.

When XRST is L, M1 continues switching until the reference voltage dividing VBH is exceeded to generate VG for starting from VBH.



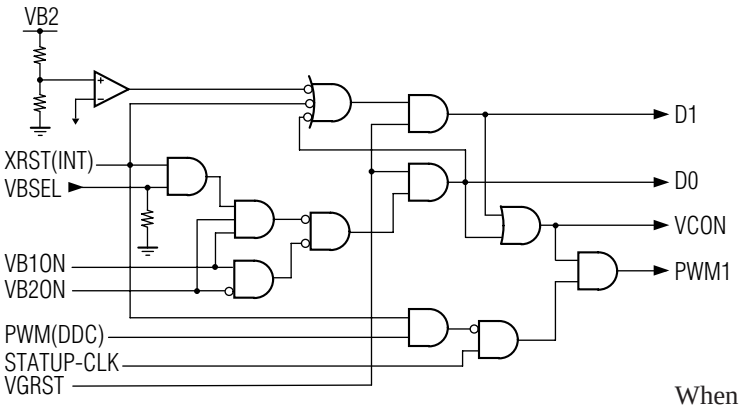
SPCK Buffer Circuit

SPCKI is negated until XRST becomes H. SPCKI is also pulled-up to VC.



Reset Circuit

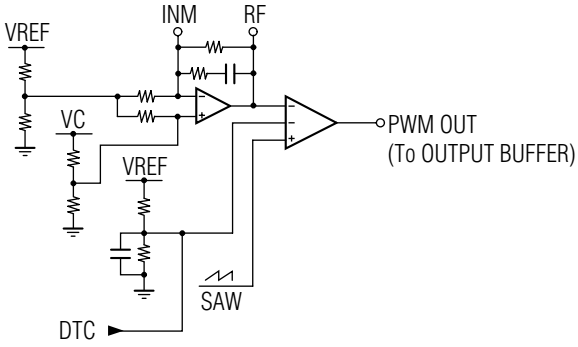
When VC reaches 88% of the expected value, the output of the comparator becomes L, M1 and M2 go OFF, and as a result XRST becomes H. The timing can also be delayed using the capacitor attached externally to CRST.



To MPC17A55

Mode Select and Output Buffer Circuit

When XRST (INT) is L, as VBSEL is negated, the D0 and D1 logics are determined according to VB1 ON and VB2 ON. Voltage is output when VGRST becomes H. If VB2 is being supplied, both D0 and D1 are set to H, and the MPC17A55 is set into the up-down mode to perform start. After starting, when XRST (INT) becomes H, if VB2 is above 3.3V, D0 is set to H and D1 is set to L to set the step-down mode. PWM1 outputs the STARTUP CLK when XRST (INT) is L.



Switching Power Supply operation Circuit

The switching power supply control circuit is composed of the error amplifier and comparator. The error amplifier extracts the error voltage from the 1/2 reference voltage of VREF and VC, and generates PWM from SAW. DTC performs the software-switching at start and at the same time, limits the PWM duty. Although the maximum duty is set to 95%, it can be changed through external settings. In addition, as MPC1830 is not equipped with the power section required for controlling the switching power supply, the MPCV17A55 or an external transistor is required.